VIPER17

RELIABILITY REPORT

Product Line :	*MV34*
See Reliability Reference Number :	*RR004216CS6080*

Reliability Report

General Information	
Product Line	*MV34 (VZ8Q+UL39)*
Product Description	*High Voltage Converter*
Product division	*I&PC*
Package	*SO16/PDIP7*
Silicon process technology	*BCD6 (UL39)* *SUPERMESH (VZ8Q)*

Locations	
Wafer fab location	*ANG MO KIO (VZ8Q) + CATANIA (UL39)*
Assembly plant location	*UTAC Thai Limited (SO16) /NANTONG FUJITSU (PDIP7)*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	29-July-15	10	A.Spiezia	Original document

Approved by

Giuseppe Capodici

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation performed on MV34 (VZ8Q+UL39) device diffused in ANG MO KIO (VZ8Q) + CATANIA (UL39) and assembled in SO16/PDIP7 in UTAC Thai Limited (SO16) /NANTONG FUJITSU (PDIP7)

According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- High Temperature Reverse Bias

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Pressure Pot
- High Temperature Storage Life
- Temperature Humidity Bias

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the positive results of the trials performed, the MV34 (VZ8Q+UL39) diffused in ANG MO KIO (VZ8Q) + CATANIA (UL39) and assembled in SO16 (in UTAC Thai Limited) and PDIP7 (in NANTONG FUJITSU) can be qualified from reliability viewpoint.

2.3 Traceability

Wafer fab information UL39	
Wafer fab manufacturing location	*CATANIA*
Wafer diameter	*8 inches*
Wafer thickness	*375µm*
Silicon process technology	*BCD6 3M*
Die finishing back side	*RAW SILICON*
Die size	*1320x1112µm*
Bond pad metallization layers	*AlCu*
Passivation	*Polymide*
Metal levels	*3*

Wafer fab information VZ8Q	
Wafer fab manufacturing location	*AMJ9*
Wafer diameter	*6 inches*
Wafer thickness	*280µm*
Silicon process technology	*SUPERMESH*
Die finishing back side	*Ti-Ni-Au*
Die size	*2650x1290µm*
Bond pad metallization layers	*AlSi*
Passivation	*SiN*
Metal levels	*1*

Assembly Information SO16N	
Assembly plant location	*UTAC Thai Limited*
Package description	*SO16N*
Molding compound	*G605*
Wires bonding materials/diameters	*Au/1mil*
Die attach material	*8200T*
Lead solder material	*Ni/Pd/Au PPF*

Assembly Information PDIP7	
Assembly plant location	*NANTONG Fujitsu - CHINA*
Package description	*PDIP7*
Molding compound	*8200DTA*
Wires bonding materials/diameters	*Au/1mil*
Die attach material	*8390*
Lead solder material	*Sn*

3 TESTS RESULTS SUMMARY

3.1 LOTs information

Lot ID #	Silicon Rev.	Package	Assy Plant	Comments
1	BE6	SO16	UTAC Thai Limited	
2	BE6	PDIP7	NANTONG FUJITSU- CHINA	
3	BD6	PDIP7	NANTONG FUJITSU- CHINA	
4	BD6	PDIP7	NANTONG FUJITSU- CHINA	
5	BD6	PDIP7	NANTONG FUJITSU- CHINA	
6	Equivalent test vehicle	SO16	UTAC Thai Limited	
7	Equivalent test vehicle	SO16	UTAC Thai Limited	
8	Equivalent test vehicle	SO16	UTAC Thai Limited	

3.2 Test plan and results summary

Die Oriented Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
HTOL	High Temperature Operating Life (Dymamic)						
		Tj=150°C Vdd=22V	-	0/77	-	168h	
			-	-	0/78	1000h	
HTRB	High Temperature Reverse Bias (Static)						
		Tj=150°C Vdd=22V	0/77	0/77	-	168h	
			-	-	0/77	1000h	

Package Oriented Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 3	Lot 4	Lot 5		
THB	Temperature Humidity Bias (Static)						
		Ta=85°c/85%R.H. Vdd=22V	0/25	0/25	0/25	1000h	
AC	Pressure Pot						
		121°C 2atm	0/25	0/25	0/25	168h	
TC	Temperature Cycling						
		Temp. range: -65/+150°C	0/25	0/25	0/25	500cy	
HTSL	High Temperature Storage Life (No bias)						
	No Bias	Tamb=150°C	0/25	0/25	0/25	1000h	

Package Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 6	**Lot 7**	**Lot 8**		
PC	Pre-Conditioning: Moisture sensitivity level 3						
	PC before	**192h 30°C/60% - 3 reflow PBT 260°C**	**0/100**	**0/100**	**0/100**	**1000h**	
AC	Pressure Pot						
	PC before	**121°C 2atm**	**0/25**	**0/25**	**0/25**	**96h**	
TC	Temperature Cycling						
	PC before	**Temp. range: -50/+150°C**	**0/25**	**0/25**	**0/25**	**1000cy**	
HTSL	High Temperature Storage Life (No bias)						
	No Bias	**Tamb=150°C**	**0/25**	**0/25**	**0/25**	**1000h**	
THB	Temperature Humidity Bias (Static)						
	PC before	**Ta=85°C 85% RH Vdd=22V**	**0/25**	**0/25**	**0/25**	**1000h**	

Electrical Characterization Tests					
Test	**Method**	**Conditions**	**Failure/SS**	**Duration**	**Note**
			Lot 2		
ESD	Electro Static Discharge				
	Human Body Model	**+/- 4kV**	**0/3**		
	Machine Model	**+/- 200V**	**0/3**		
	Charge Device Model	**+/- 1.5KV**	**0/3**		
LU	Latch-Up				
	Over-voltage and Current Injection	**Tamb=85°C Jedec78**	**0/6**		

4 TESTS DESCRIPTION & DETAILED RESULTS

4.1 Die oriented tests

4.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electro migration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

4.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

4.2 Package oriented tests

4.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption.
The purpose is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

The read-outs flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing @ Ta=25°C.

4.2.2 High Temperature Storage Life

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

4.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)

4.2.4 Pressure Pot

The purpose of this test is to point out critical water entry path with consequent electrochemical and galvanic corrosion effects.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

4.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

4.3 Electrical Characterization Tests

4.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

4.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011

VIPER17

Energy saving VIPerPlus: HV switching regulator for flyback converter

Datasheet - production data

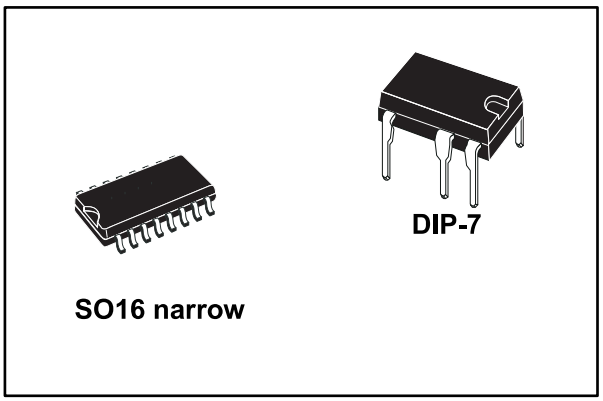
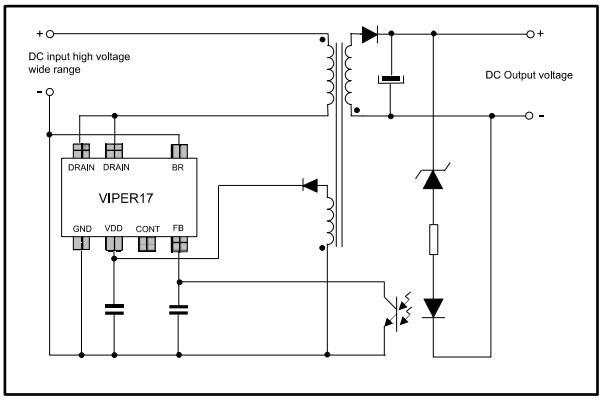


Figure 1: Typical topology



Features

- 800 V avalanche rugged power section
- PWM operation with frequency jittering for low EMI
- Operating frequency:
  - 60 kHz for L type
  - 115 kHz for H type
- Standby power < 30 mW at 265 V_{AC}
- Limiting current with adjustable set point
- Adjustable and accurate overvoltage protection
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteresis thermal shutdown

Applications

- Adapters for PDA, camcorders, shavers, cellular phones, videogames
- Auxiliary power supply for LCD/PDP TV, monitors, audio systems, computer, industrial systems, LED driver, No el-cap LED driver
- SMPS for set-top boxes, DVD players and recorders, white goods

Description

The device is an off-line converter with an 800 V rugged power section, a PWM control, two levels of overcurrent protection, overvoltage and overload protections, hysteresis thermal protection, soft-start and safe auto-restart after any fault condition removal. The burst mode operation and the device's very low consumption meet the standby energy saving regulations.

Advance frequency jittering reduces EMI filter cost. Brown-out function protects the switch mode power supply when the rectified input voltage level is below the normal minimum level specified for the system. The high voltage startup circuit is embedded in the device.

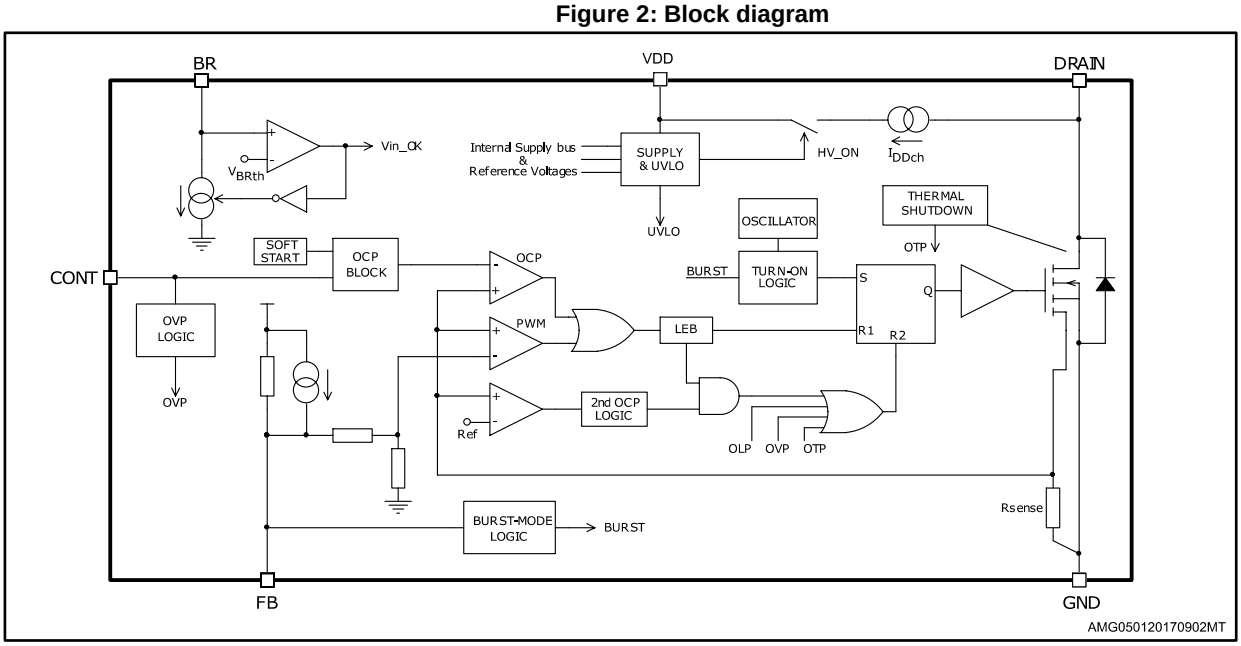
Table 1: Device summary

Order code	Package	Packing
VIPER17LN / VIPER17HN	DIP-7	Tube
VIPER17HD / VIPER17LD	SO16 narrow	Tube
VIPER17HDTR / VIPER17LDTR		Tape and reel

Contents

1 Block diagram

Figure 2: Block diagram



2 Typical power

Table 2: Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter (1)	Open frame (2)	Adapter (1)	Open frame (2)
	9 W	10 W	5 W	6 W

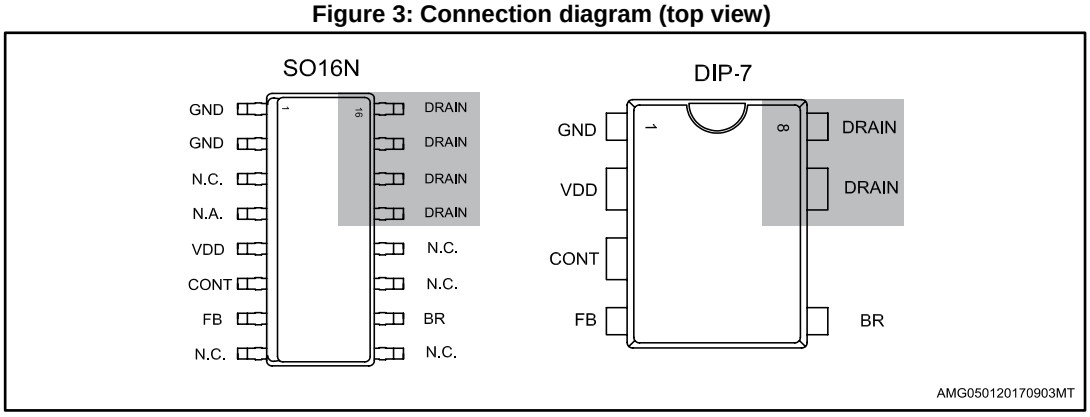
Notes:

(1)Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.

(2)Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

3 Pin settings

Figure 3: Connection diagram (top view)



The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3: Pin description

Pin n.		Name	Function
DIP-7	SO16		
1	1...2	GND	This pin represents the device ground and the source of the power section.
-	4	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity, is highly recommended connect it to GND (pin 1-2).
2	5	VDD	Supply voltage of the control section. This pin also provides the charging current of the external capacitor during startup time.
3	6	CONT	Control pin. The following functions can be selected: 1. current limit set point adjustment. The internal set default value of the cycle-by-cycle current limit can be reduced by connecting to ground an external resistor. 2. output voltage monitoring. A voltage exceeding V_{OVP} threshold (see *Table 8: "Controller section "*) shuts the IC down reducing the device consumption. This function is strobed and digitally filtered for high noise immunity.
4	7	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates the burst-mode operation. A level close to the threshold V_{FBlin} means that we are approaching the cycle-by-cycle over-current set point.
5	10	BR	Brownout protection input with hysteresis. A voltage below the threshold V_{BRth} shuts down (not latch) the device and lowers the power consumption. Device operation restarts as the voltage exceeds the threshold $V_{BRth} + V_{BRhyst}$. It can be connected to ground when not used.
7,8	13-16	DRAIN	High voltage drain pin. The built-in high voltage switched startup bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4: Absolute maximum ratings

Symbol	Pin (DIP-7)	Parameter	Value		Unit
			Min.	Max.	
V_{DRAIN}	7, 8	Drain-to-source (ground) voltage		800	V
E_{AV}	7, 8	Repetitive avalanche energy (limited by T_J = 150 °C)		2	mJ
I_{AR}	7, 8	Repetitive avalanche current (limited by T_J = 150 °C)		1	A
I_{DRAIN}	7, 8	Pulse drain current		2.5	A
V_{CONT}	3	Control input pin voltage (with I_{CONT} = 1 mA)	-0.3	Self limited	V
V_{FB}	4	Feed-back voltage	-0.3	5.5	V
V_{BR}	5	Brown-out input pin voltage (with I_{BR} = 0.5 mA)	-0.3	Self limited	V
V_{DD}	2	Supply voltage (I_{DD} = 25 mA)	-0.3	Self limited	V
I_{DD}	2	Input current		25	mA
P_{TOT}		Power dissipation at T_A < 40 °C (DIP-7)		1	W
		Power dissipation at T_A < 60 °C (SO16N)		1	W
T_J		Operating junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C
$ESD_{(HBM)}$	1 to 8	Human body model		4	kV
$ESD_{(CDM)}$	1 to 8	Charge device model		1.5	kV

4.2 Thermal data

Table 5: Thermal data

Symbol	Parameter	Max. value SO16N	Max. value DIP-7	Unit
R_{thJP}	Thermal resistance junction pin (dissipated power = 1 W)	35	40	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W)	110	110	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W) (1)	80	90	°C/W

Notes:

(1)When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq in) of Cu (35 µm thick).

4.3 Electrical characteristics

(T_J = -25 to 125 °C, V_{DD} = 14 V)[a]

Table 6: Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Break-down voltage	I_{DRAIN} = 1 mA V_{FB} = GND T_J = 25 °C	800			V
I_{OFF}	OFF state drain current	V_{DRAIN} = 640 V V_{FB} = GND			60	µA
		V_{DRAIN} = 800 V V_{FB} = GND			75	µA
$R_{DS(on)}$	Drain-source on state resistance	I_{DRAIN} = 0.2 A, V_{FB} = 3 V V_{BR} = GND, T_J = 25 °C		20	24	Ω
		I_{DRAIN} = 0.2 A V_{FB} = 3 V V_{BR} = GND T_J = 125 °C		40	48	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		10		pF

Table 7: Supply section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch}	Startup charging current	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 4 V	-2	-3	-4	mA
		V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 4 V after fault.	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 20 mA	23.5			V
V_{DDon}	V_{DD} startup threshold	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND	13	14	15	V
V_{DDoff}	V_{DD} under voltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND	4	4.5	5	V

[a] Adjust V_{DD} above V_{DDon} startup threshold before settings to 14 V.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current						
I_{DD0}	Operating supply current, not switching	V_{FB} = GND F_{SW} = 0 kHz V_{BR} = GND, V_{DD} = 10 V			0.9	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V F_{SW} = 60 kHz			1.8	mA
		V_{DRAIN} = 120 V F_{SW} = 115 kHz			2	mA
I_{DD_FAULT}	Operating supply current, with protection tripping				400	µA
I_{DD_OFF}	Operating supply current with $V_{DD} < V_{DD\_off}$	V_{DD} = 7 V			270	µA

Table 8: Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Feed-back pin						
V_{FBolp}	Overload shut down threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.2	3.3	3.4	V
V_{FBbm}	Burst mode threshold	Voltage falling	0.4	0.45	0.6	V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		50		mV
I_{FB}	Feed-back sourced current	V_{FB} = 0.3 V	-150	-200	-280	uA
		3.3 V < V_{FB} < 4.8 V		-3		uA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB} < 3.3 V	12		19	kΩ
H_{FB}	ΔV_{FB} / ΔI_D		3		8	V/A
CONT pin						
VCONT_l	Low level clamp voltage	I_{CONT} = -100 µA		0.5		V
VCONT_h	High level clamp voltage	I_{CONT} = 1 mA	5	5.5	6	V
Current limitation						
I_{Dlim}	Max drain current limitation (1)	V_{FB} = 4 V I_{CONT} = -10 µA T_J = 25 °C	0.38	0.4	0.42	A
t_{SS}	Soft-start time			8.5		ms
T_{ON_MIN}	Minimum turn ON time		220	400	480	ns
td	Propagation delay	(2)		100		ns
t_{LEB}	Leading edge blanking	(2)		300		ns
I_{D_BM}	Peak drain current during burst mode	V_{FB} = 0.6 V		90		mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Oscillator section						
F_{OSC}	VIPER17L	V_{DD} = operating voltage range V_{FB} = 1 V	54	60	66	kHz
	VIPER17H		103	115	127	kHz
FD	Modulation depth	VIPER17L		±4		kHz
		VIPER17H		±8		kHz
FM	Modulation frequency			250		Hz
D_{MAX}	Maximum duty cycle		70		80	%
Overcurrent protection (2nd OCP)						
I_{DMAX}	Second over current threshold	(2)		0.6		A
Overvoltage protection						
V_{OVP}	Overvoltage protection threshold		2.7	3	3.3	V
T_{STROBE}	Overvoltage protection strobe time			2.2		µs
Brown out protection						
V_{BRth}	Brown out threshold	Voltage falling	0.41	0.45	0.49	V
V_{BRhyst}	Voltage hysteresis above V_{BRth}			50		mV
I_{BRhyst}	Current hysteresis		7		12	µA
$V_{BRclamp}$	Clamp voltage	I_{BR} = 250 µA		3		V
V_{DIS}	Brown out disable voltage		50		150	mV
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(2)	150	160		°C
T_{HYST}	Thermal shutdown hysteresis	(2)		30		°C

Notes:

(1)I_{Dlim} @ V_{DD} lower than 10 V can range between -5 % and +15 %.

(2)Specification assured by design, characterization and statistical correlation.

Figure 4: Minimum turn-on time test circuit

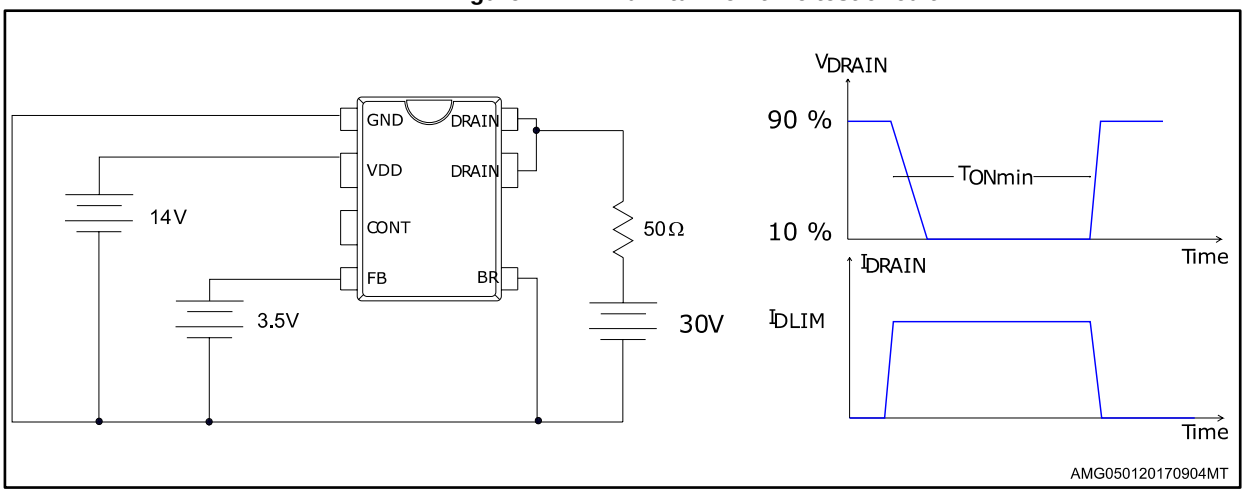


Figure 5: Brown out threshold test circuit

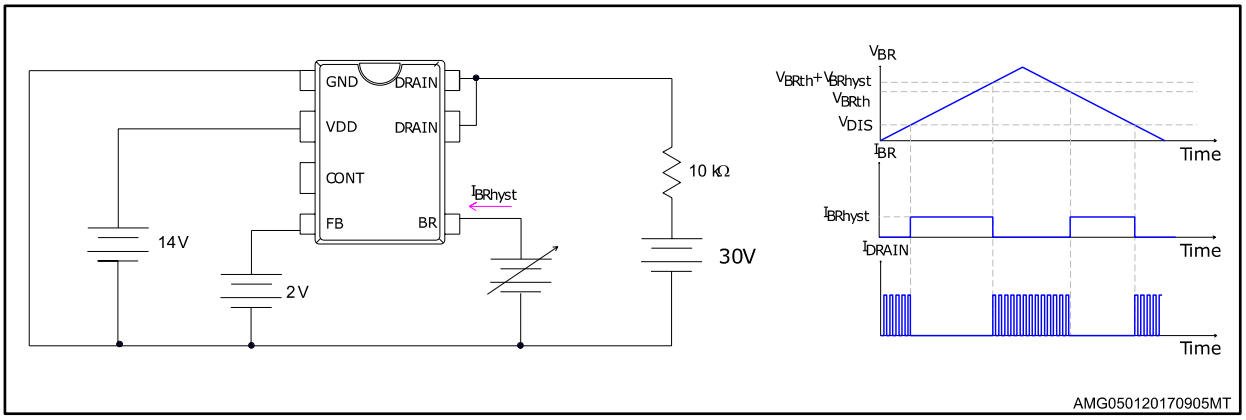
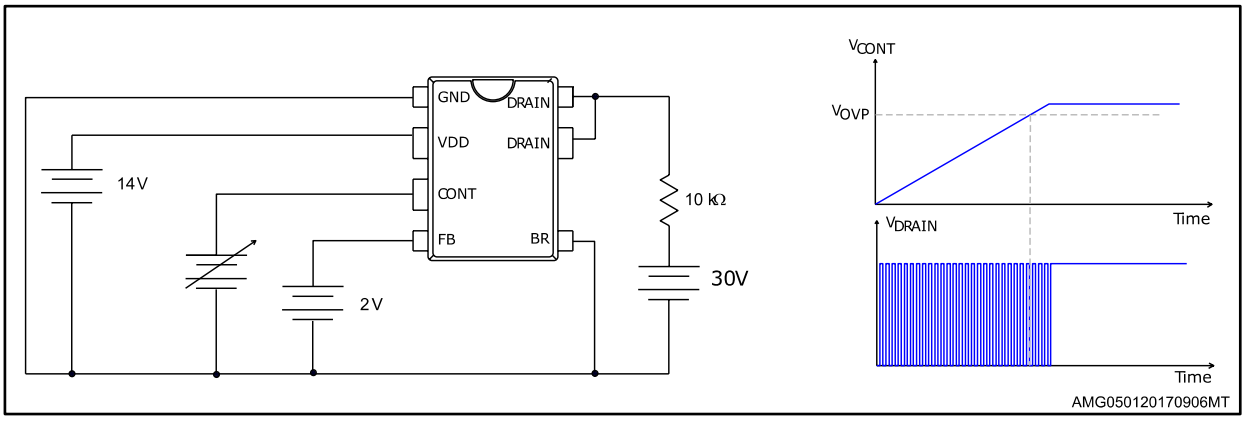


Figure 6: OVP threshold test circuit



Adjust V_{DD} above V_{DDon} startup threshold before settings to 14 V.

5 Typical electrical characteristics

Figure 7: Current limit vs T_J

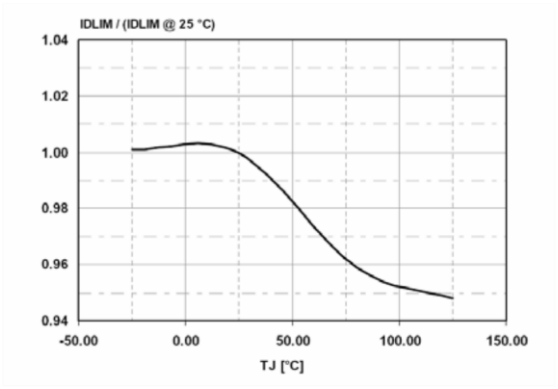


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Figure 8: Switching frequency vs T_J

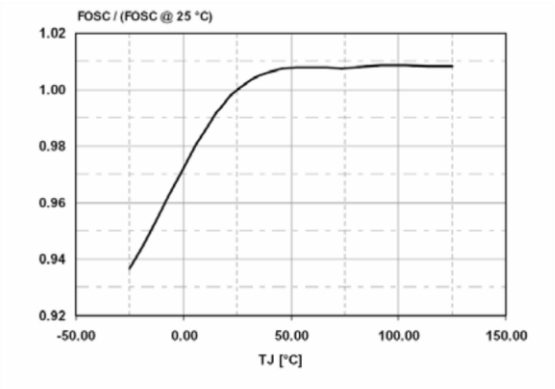

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Figure 9: Drain start voltage vs T_J

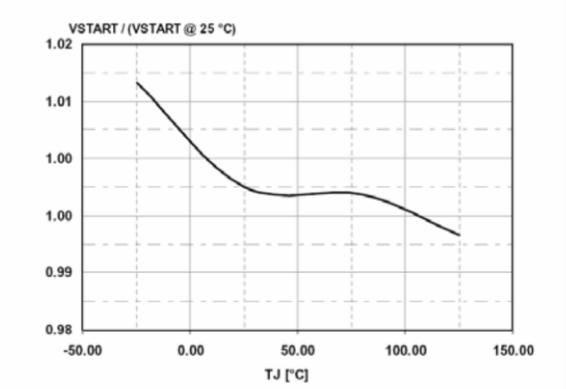

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Figure 10: HFB vs T_J

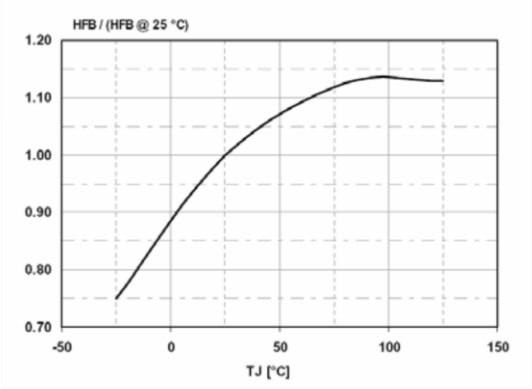

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Figure 11: Brown out threshold vs T_J

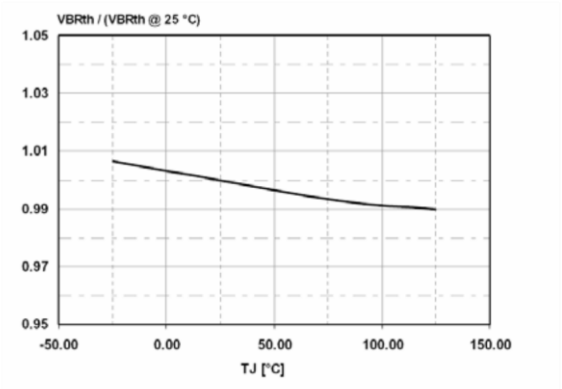

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Figure 12: Brown out hysteresis vs T_J

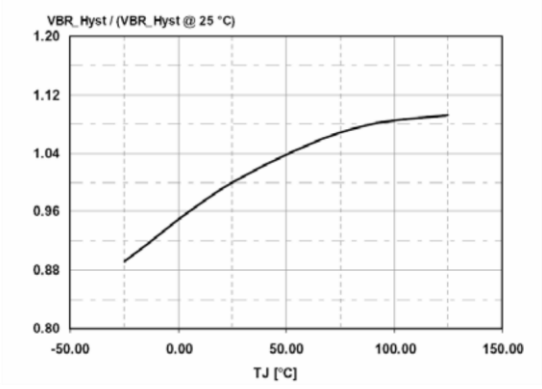

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Figure 13: Brown out hysteresis current vs T_J

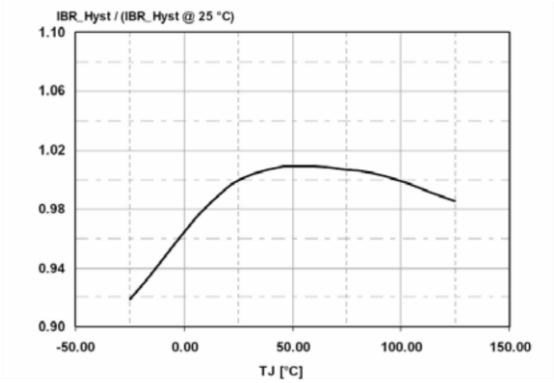

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Figure 14: Operating supply current (no switching) vs T_J

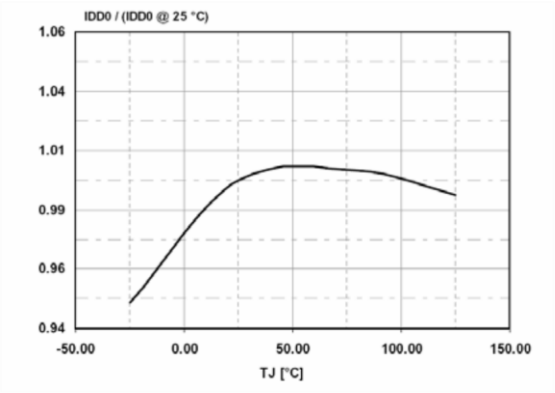

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Figure 15: Operating supply current (switching) vs T_J

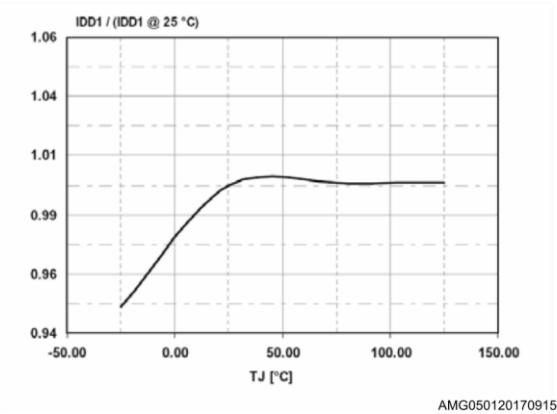

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Figure 16: Current limit vs R_{LIM}

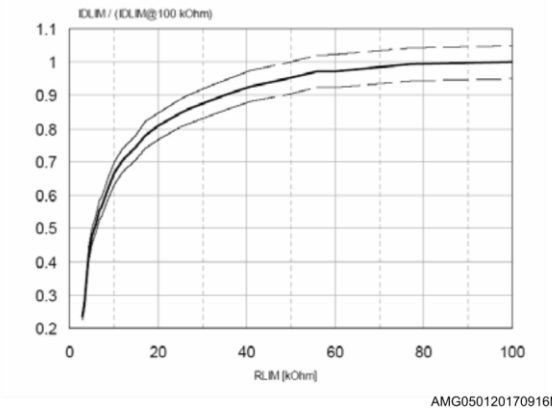

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Figure 17: Power MOSFET on-resistance vs T_J

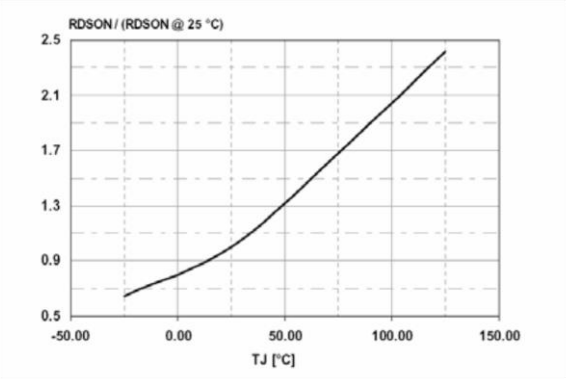

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Figure 18: Power MOSFET break down voltage vs T_J

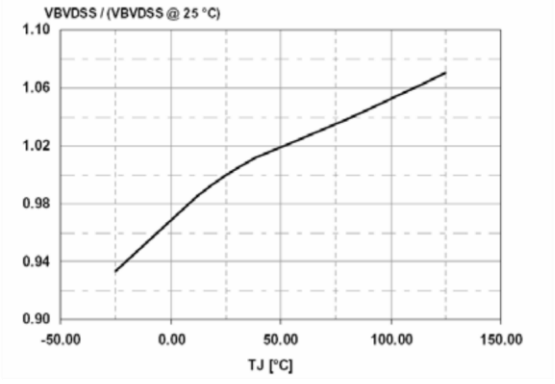

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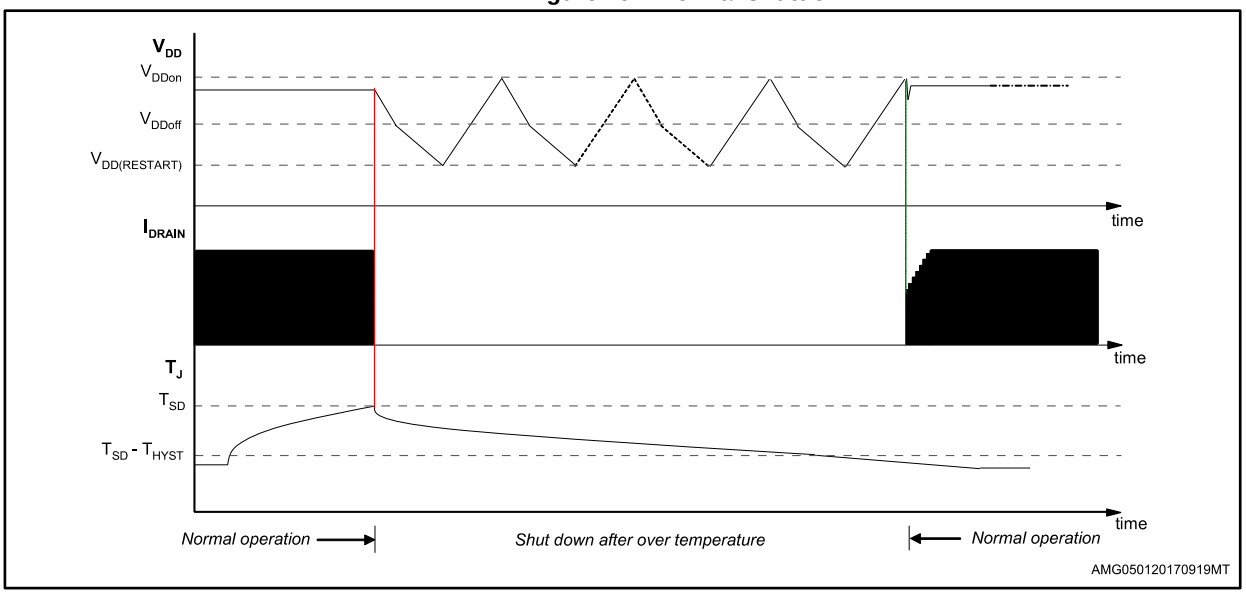
Figure 19: Thermal shutdown



6 Typical circuit

Figure 20: Min-features flyback application

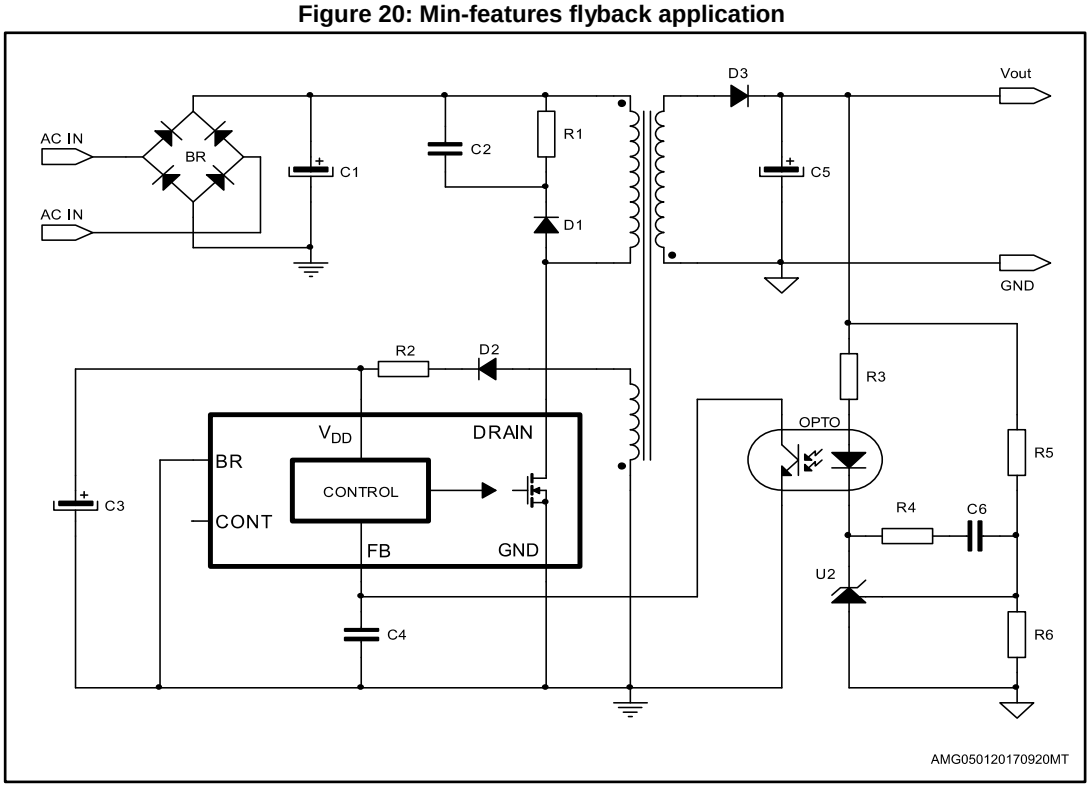
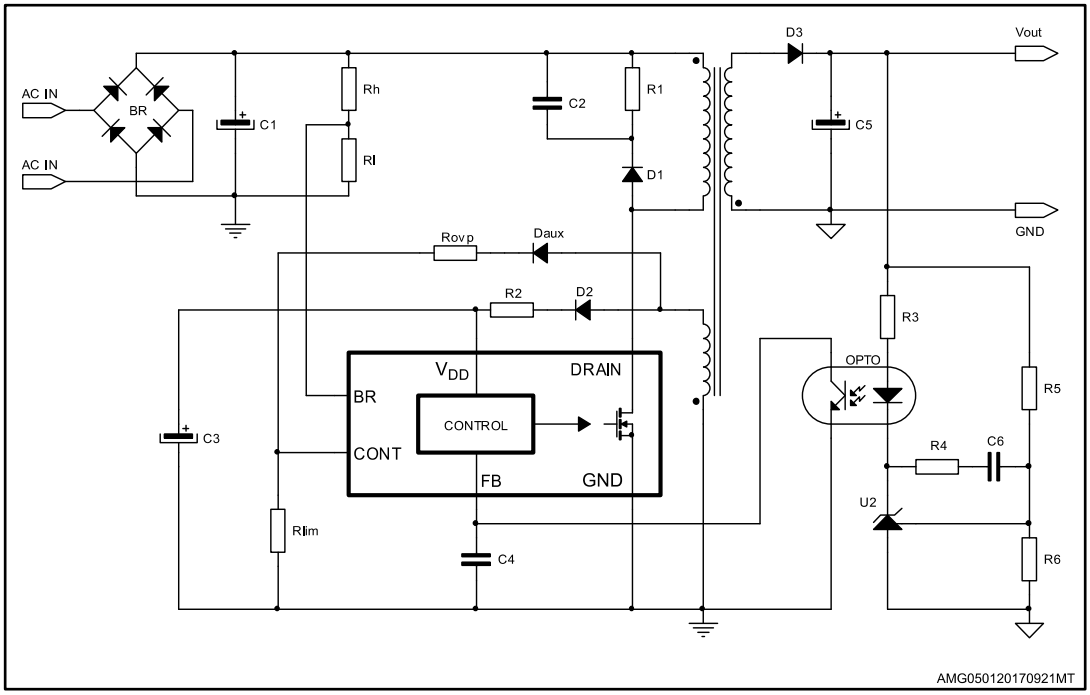


Figure 21: Full-features flyback application



7 Operation descriptions

VIPER17 is a high-performance low-voltage PWM controller chip with an 800 V, avalanche rugged power section.

The controller includes: the oscillator with jittering feature, the startup circuits with soft-start feature, the PWM logic, the current limit circuit with adjustable set point, the second over current circuit, the burst mode management, the brown-out circuit, the UVLO circuit, the auto-restart circuit and the thermal protection circuit.

The current limit set-point is set by the CONT pin. The burst mode operation guaranties high performance in the stand-by mode and helps in the energy saving norm accomplishment.

All the fault protections are built in auto restart mode with very low repetition rate to prevent IC's over heating.

7.1 Power section and gate driver

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a BV_{DSS} of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the Power section cannot be turned on accidentally.

7.2 High voltage startup generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{DRAIN_START} threshold, 80 V_{DC} typically. When the HV current generator is ON, the I_{DDch} current (3 mA typical value) is delivered to the capacitor on the V_{DD} pin. In case of auto restart mode after a fault event, the I_{DDch} current is reduced to 0.6 mA, in order to have a slow duty cycle during the restart phase.

7.3 Power-up and soft-startup

If the input voltage rises up till the device start threshold, V_{DRAIN_START}, the V_{DD} voltage begins to grow due to the I_{DDch} current (see *Table 7: "Supply section "*) coming from the internal high voltage startup circuit. If the V_{DD} voltage reaches V_{DDon} threshold (see *Table 7: "Supply section "*) the power MOSFET starts switching and the HV current generator is turned OFF. See *Figure 23: "Timing diagram: normal power-up and power-down sequences"*.

The IC is powered by the energy stored in the capacitor on the VDD pin, C_{VDD}, until when the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

C_{VDD} capacitor must be sized enough to avoid fast discharge and keep the needed voltage value higher than V_{DDoff} threshold. In fact, a too low capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used for the V_{DD} capacitor calculation:

Equation 1

$$C_{VDD} = \frac{I_{DDch} \times t_{SSaux}}{V_{DDon} - V_{DDoff}}$$

The t_{SSaux} is the time needed for the steady state of the auxiliary voltage. This time is estimated by applicator according to the output stage configurations (transformer, output capacitances, etc.).

During the converter startup time, the drain current limitation is progressively increased to the maximum value. In this way the stress on the secondary diode is considerably reduced. It also helps to prevent transformer saturation. The soft-start time lasts 8.5 ms and the feature is implemented for every attempt of startup converter or after a fault.

Figure 22: IDD current during startup and burst mode

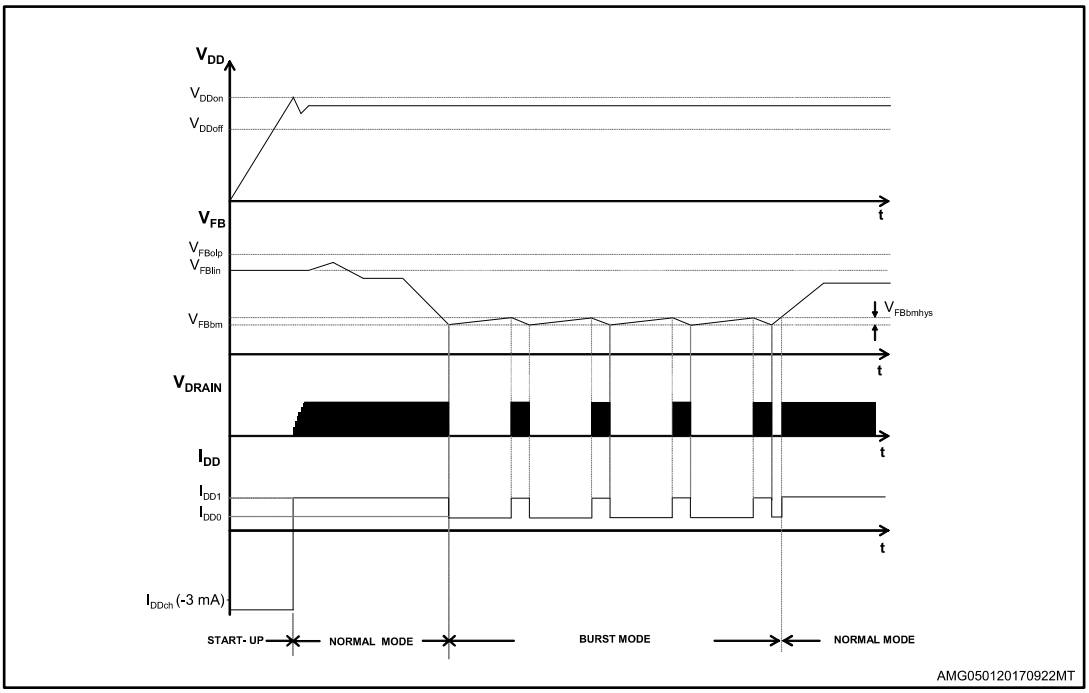


Figure 23: Timing diagram: normal power-up and power-down sequences

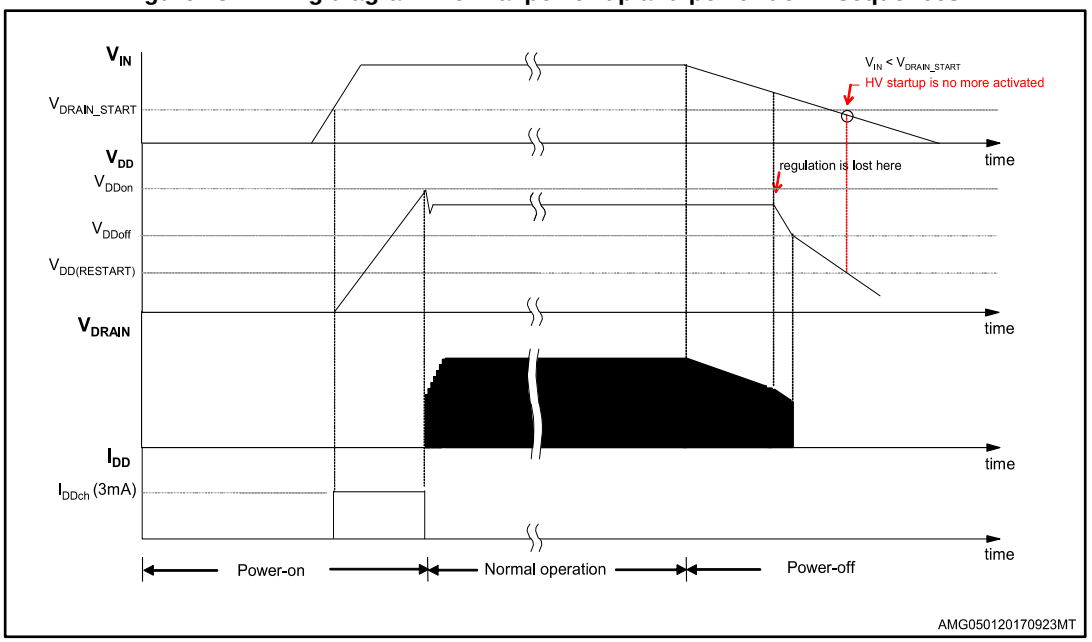
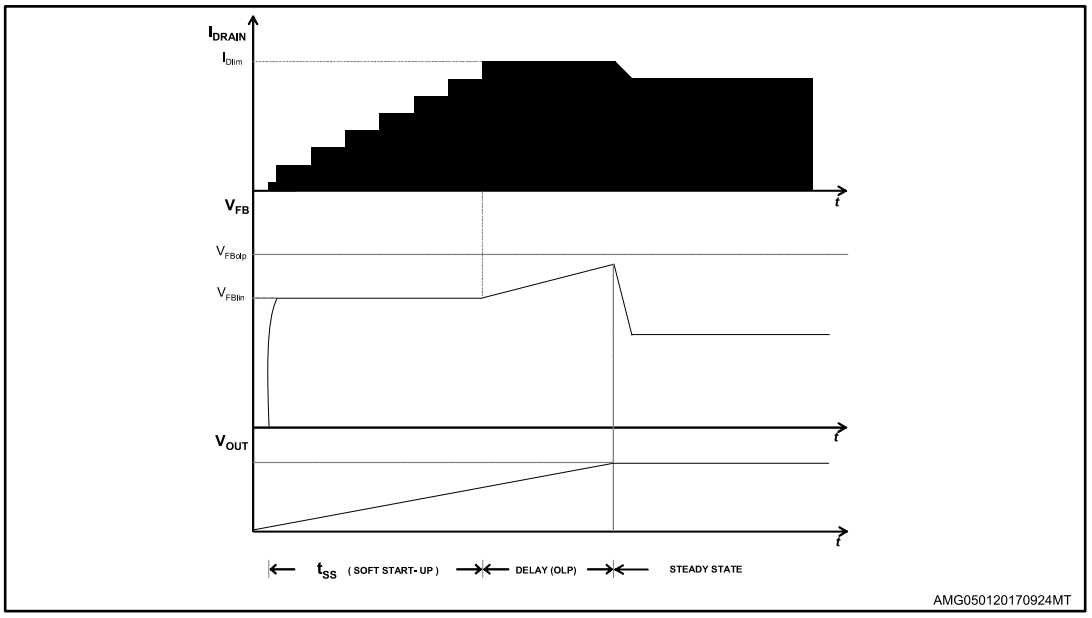


Figure 24: Soft-start: timing diagram



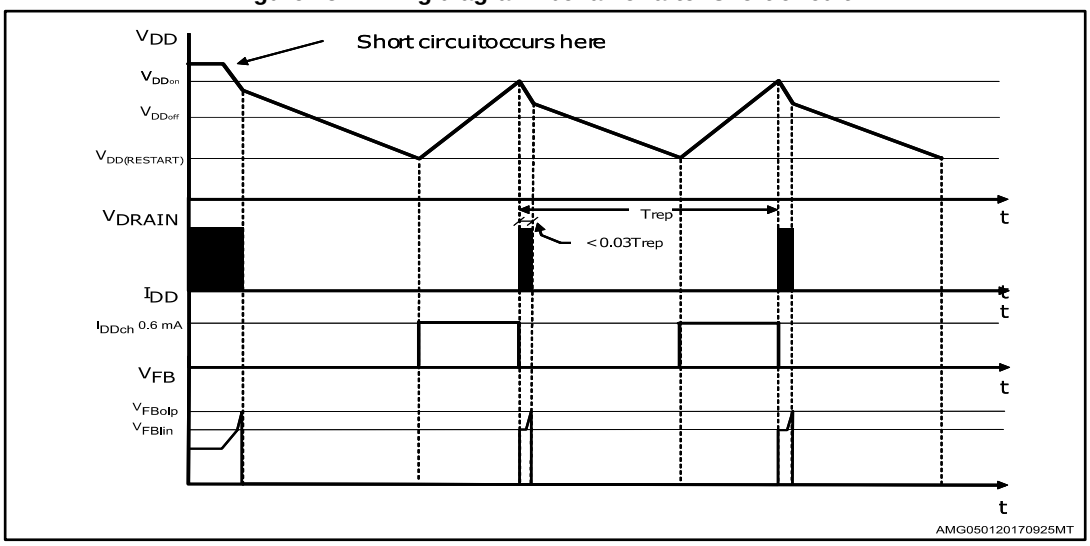
7.4 Power down operation

At converter power down, the system loses regulation as soon as the input voltage is so low that the peak current limitation is reached. The V_{DD} voltage drops and when it falls below the V_{DDoff} threshold (see *Table 7: "Supply section "*) the power MOSFET is switched OFF, the energy transfers to the IC interrupted and consequently the V_{DD} voltages decreases, *Figure 23: "Timing diagram: normal power-up and power-down sequences"*. Later, if the V_{IN} is lower than V_{DRAIN_START} (see *Table 7: "Supply section "*), the startup sequence is inhibited and the power down completed. This feature is useful to prevent converter's restart attempts and ensures monotonic output voltage decay during the system power down.

7.5 Auto restart operation

If after a converter power down, the V_{IN} is higher than $V_{DRAIN\_START,}$ the startup sequence is not inhibited and will be activated only when the V_{DD} voltage drops down the $V_{DD(RESTART)}$ threshold (see *Table 7: "Supply section "*). This means that the HV startup current generator restarts the V_{DD} capacitor charging only when the V_{DD} voltage drops below $V_{DD(RESTART)}$. The scenario above described is for instance a power down because of a fault condition. After a fault condition, the charging current, I_{DDch}, is 0.6 mA (typ.) instead of the 3 mA (typ.) of a normal startup converter phase. This feature together with the low $V_{DD(RESTART)}$ threshold ensures that, after a fault, the restart attempts of the IC has a very long repetition rate and the converter works safely with extremely low power throughput. The *Figure 25: "Timing diagram: behavior after short circuit"* shows the IC behavioral after a short circuit event.

Figure 25: Timing diagram: behavior after short circuit



7.6 Oscillator

The switching frequency is internally fixed to 60 kHz or 115 kHz. In both case the switching frequency is modulated by approximately ±4 kHz (60 kHz version) or ±8 kHz (115 kHz version) at 250 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of side-band harmonics having the same energy on the whole but smaller amplitudes.

7.7 Current mode conversion with adjustable current limit set point

The device is a current mode converter: the drain current is sensed and converted in voltage that is applied to the non inverting pin of the PWM comparator. This voltage is compared with the one on the feed-back pin through a voltage divider on cycle by cycle basis.The VIPER17 has a default current limit value, I_{DLIM}, that the designer can adjust according the electrical specification, by the R_{LIM} resistor connected to the CONT see *Figure 16: "Current limit vs RLIM"*.

The CONT pin has a minimum current sunk needed to activate the I_{DLIM} adjustment: without R_{LIM} or with high R_{LIM} (i.e. 100 KΩ) the current limit is fixed to the default value (see I_{DLIM}, *Table 8: "Controller section "*).

7.8 Overvoltage protection (OVP)

The VIPER17has integrated the logic for the monitor of the output voltage using as input signal the voltage V_{CONT} during the OFF time of the power MOSFET. This is the time when the voltage from the auxiliary winding tracks the output voltage, through the turn ratio

$\frac{N_{AUX}}{N_{SEC}}$

The CONT pin has to be connected to the auxiliary winding through the diode D_{OVP} and the resistors R_{OVP} and R_{LIM} as shows the *Figure 27: "CONT pin configuration"*. When, during the OFF time, the voltage V_{CONT} exceeds, four consecutive times, the reference voltage V_{OVP} (see *Table 8: "Controller section "*) the overvoltage protection will stop the power MOSFET and the converter enters the auto-restart mode.

In order to bypass the noise immediately after the turn off of the power MOSFET, the voltage V_{CONT} is sampled inside a short window after the time T_{STROBE}, see *Table 8: "Controller section "* and the *Figure 26: "OVP timing diagram"*. The sampled signal, if higher than V_{OVP}, trigger the internal OVP digital signal and increments the internal counter. The same counter is reset every time the signal OVP is not triggered in one oscillator cycle.

Referring to the *Figure 21: "Full-features flyback application"*, the resistors divider ratio k_{OVP} will be given by:

Equation 2

$$K_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUTOVP} + V_{DSEC}) - V_{DAUX}}$$

Equation 3

$$K_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}}$$

Where:

- V_{OVP} is the OVP threshold (see *Table 8: "Controller section "*)
- $V_{OUT\ OVP}$ is the converter output voltage value to activate the OVP (set by designer)
- N_{AUX} is the auxiliary winding turns
- N_{SEC} is the secondary winding turns
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage
- R_{OVP} together R_{LIM} make the output voltage divider

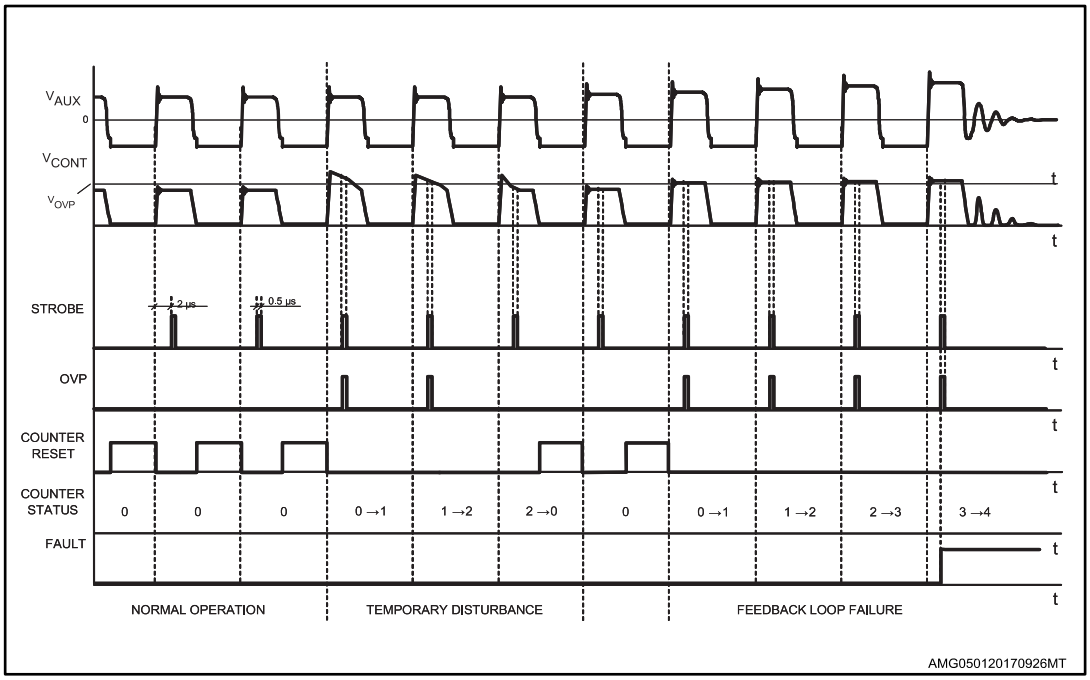
Than, fixed R_{LIM}, according to the desired I_{DLIM}, the R_{OVP} can be calculating by:

Equation 4

$$R_{OVP} = R_{LIM} \times \frac{1 - K_{OVP}}{K_{OVP}}$$

The resistor values will be such that the current sourced and sunk by the CONT pin be within the rated capability of the internal clamp.

Figure 26: OVP timing diagram



7.9 About CONT pin

Referring to the *Figure 27: "CONT pin configuration"*, through the CONT pin, the below features can be implemented:

1. Current Limit set point
2. Over voltage protection on the converter output voltage

The *Table 9: "CONT pin configurations"* referring to the *Figure 27: "CONT pin configuration"*, lists the external components needed to activate one or plus of the CONT pin functions.

Figure 27: CONT pin configuration

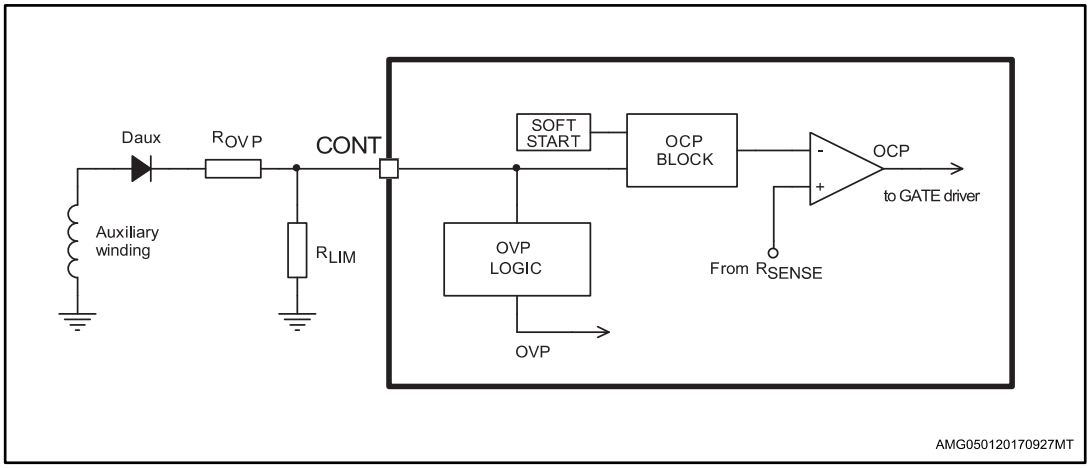


Table 9: CONT pin configurations

Function / component	R_{LIM} (1)	R_{OVP}	D_{AUX}
I_{Dlim} reduction	See *Figure 16: "Current limit vs RLIM"*	No	No
OVP	≥ 80 KΩ	See ***Equation 4***	Yes
I_{Dlim} reduction + OVP	See *Figure 16: "Current limit vs RLIM"*	See ***Equation 4***	Yes

Notes:

(1)R_{LIM} has to be fixed before of R_{OVP}.

7.10 Feed-back and overload protection (OLP)

The VIPER17 is a current mode converter: the feedback pin controls the PWM operation, controls the burst mode and actives the overload protection. *Figure 28: "FB pin configuration (minimal) "* and *Figure 29: " FB pin configuration (two poles and one zero)"* show the internal current mode structure.

With the feedback pin voltage between V_{FBbm} and V_{FBlin}, see *Table 8: "Controller section "*, the drain current is sensed and converted in voltage that is applied to the non inverting pin of the PWM comparator. See *Figure 2: "Block diagram"*.

This voltage is compared with the one on the feedback pin through a voltage divider on cycle by cycle basis. When these two voltages are equal, the PWM logic orders the switch off of the power MOSFET. The drain current is always limited to I_{Dlim} value.

In case of overload the feedback pin increases in reaction to this event and when it goes higher than V_{FBlin}, the PWM comparator is disabled and the drain current is limited to I_{Dlim} by the OCP comparator, see *Figure 2: "Block diagram"*.

When the feedback pin voltage reaches the threshold V_{FBlin} an internal current generator starts to charge the feedback capacitor (C_{FB}) and when the feedback voltage reaches the V_{FBolp} threshold, the converter is turned off and the startup phase is activated with reduced value of I_{DDch} to 0.6 mA. See *Table 7: "Supply section "*.

During the first startup phase of the converter, after the soft-startup time, t_{SS}, the output voltage could force the feedback pin voltage to rise up to the V_{FBolp} threshold that switches off the converter itself.

To avoid this event, the appropriate feedback network has to be selected according to the output load. More the network feedback fixes the compensation loop stability. The *Figure 28: "FB pin configuration (minimal) "* and *Figure 29: " FB pin configuration (two poles and one zero)"* show the two different feedback networks.

The time from the over load detection ($V_{FB} = V_{FBlin}$) to the device shutdown ($V_{FB} = V_{FBolp}$) can be calculating by C_{FB} value (see *Figure 28: "FB pin configuration (minimal) "* and *Figure 29: " FB pin configuration (two poles and one zero)"*), using the formula:

Equation 5

$$T_{OLP} - delay = C_{FB} \times \frac{V_{FBolp} - V_{FBlin}}{3\mu A}$$

In the *Figure 28: "FB pin configuration (minimal) "*, the capacitor connected to FB pin (C_{FB}) is used as part of the circuit to compensate the feedback loop but also as element to delay the OLP shut down owing to the time needed to charge the capacitor (see *Equation 5*).

After the startup time, t_{SS}, during which the feedback voltage is fixed at V_{FBlin}, the output capacitor could not be at its nominal value and the controller interpreter this situation as an over load condition. In this case, the OLP delay helps to avoid an incorrect device shut down during the startup.

Owing to the above considerations, the OLP delay time must be long enough to by-pass the initial output voltage transient and check the over load condition only when the output voltage is in steady state. The output transient time depends from the value of the output capacitor and from the load.

When the value of the C_{FB} capacitor calculated for the loop stability is too low and cannot ensure enough OLP delay, an alternative compensation network can be used and it is showed in *Figure 29: " FB pin configuration (two poles and one zero)"*.

Using this alternative compensation network, two poles (f_{PFB}, f_{PFB1}) and one zero (f_{ZFB}) are introduced by the capacitors C_{FB} and C_{FB1} and the resistor R_{FB1}.

The capacitor C_{FB} introduces a pole (f_{PFB}) at higher frequency than f_{ZB} and f_{PFB1}. This pole is usually used to compensate the high frequency zero due to the ESR (Equivalent Series Resistor) of the output capacitance of the fly-back converter.

The mathematical expressions of these poles and zero frequency, considering the scheme in *Figure 29: " FB pin configuration (two poles and one zero)"* are reported by the equations below:

Equation 6

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot R_{FB1}}$$

Equation 7

$$f_{PFB1} = \frac{R_{FB(DYN)} + R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot \left(R_{FB(DYN)} \cdot R_{FB1}\right)}$$

Equation 8

$$f_{PFB1} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot \left(R_{FB1} + R_{FB(DYN)}\right)}$$

The $R_{FB(DYN)}$ is the dynamic resistance seen by the FB pin.

The C_{FB1} capacitor fixes the OLP delay and usually C_{FB1} results much higher than C_{FB}. The *Equation 5* can be still used to calculate the OLP delay time but C_{FB1} has to be considered instead of C_{FB}. Using the alternative compensation network, the designer can satisfy, in all case, the loop stability and the enough OLP delay time alike.

Figure 28: FB pin configuration (minimal)

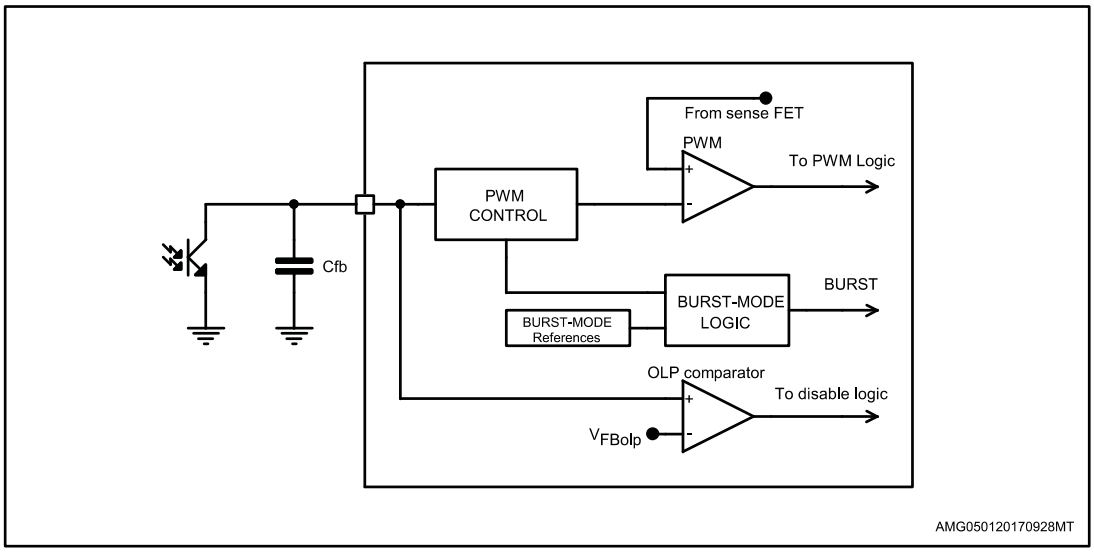
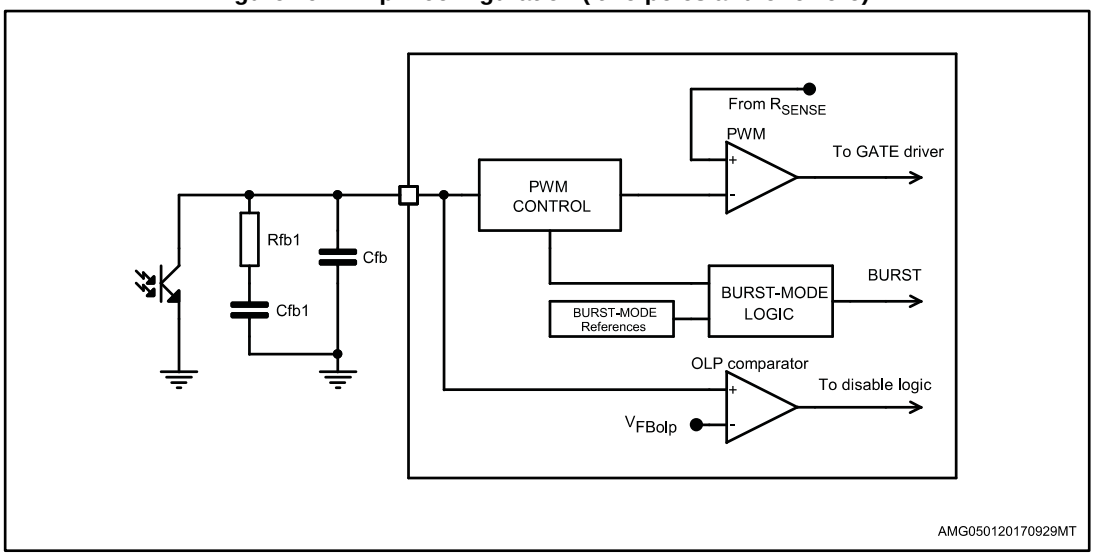


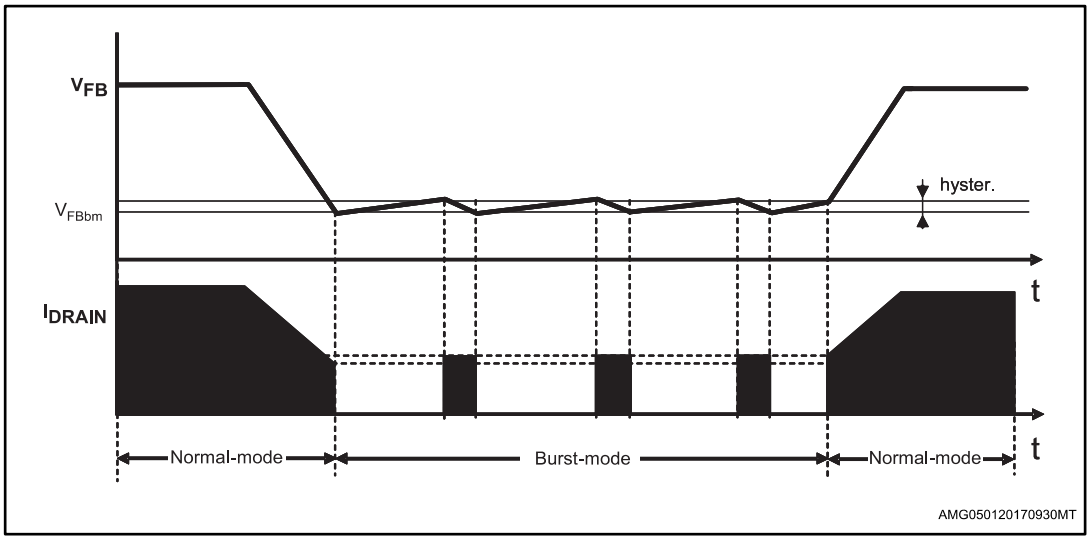
Figure 29: FB pin configuration (two poles and one zero)



7.11 Burst-mode operation at no load or very light load

When the load decrease the feedback loop reacts lowering the feedback pin voltage. If it falls down the burst mode threshold, V_{FBbm}, the power MOSFET is not more allowed to be switched on. After the MOSFET stops, as a result of the feedback reaction to the energy delivery stop, the feedback pin voltage increases and exceeding the level, $V_{FBbm} + V_{FBbmhys}$, the power MOSFET starts switching again. The burst mode thresholds are reported on *Table 8: "Controller section "* and *Figure 30: "Burst mode timing diagram, light load management"* shows this behavior. Systems alternates period of time where power MOSFET is switching to period of time where power MOSFET is not switching; this device working mode is the burst mode. The power delivered to output during switching periods exceeds the load power demands; the excess of power is balanced from not switching period where no power is processed. The advantage of burst mode operation is an average switching frequency much lower then the normal operation working frequency, up to some hundred of hertz, minimizing all frequency related losses. During the burst-mode the drain current peak is clamped to the level, I_{D_BM}, reported on *Table 8: "Controller section "*.

Figure 30: Burst mode timing diagram, light load management



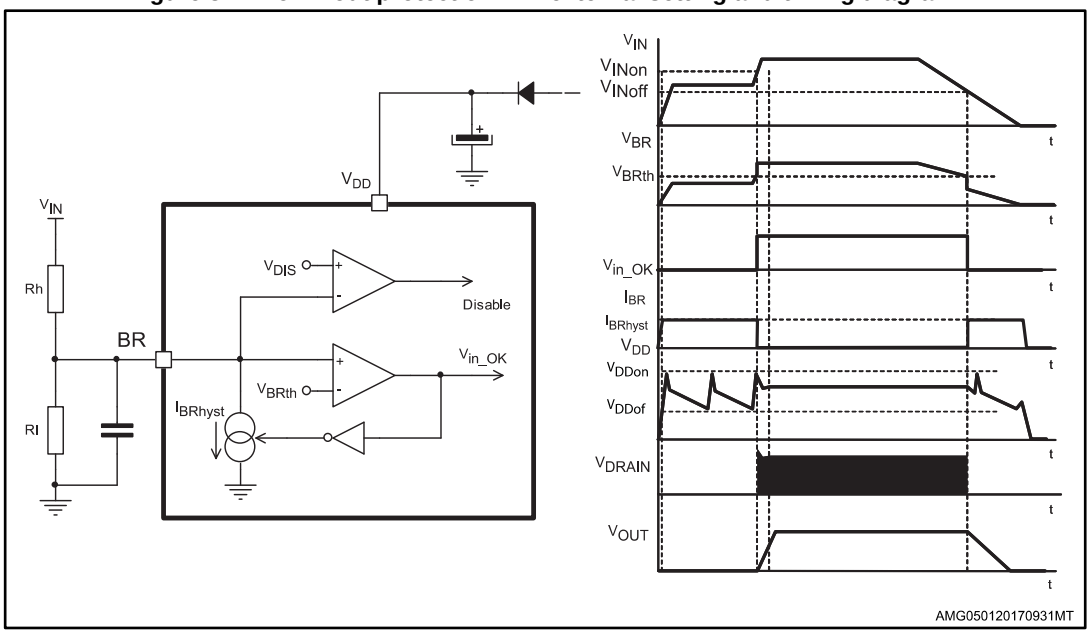
7.12 Brown-out protection

Brown-out protection is a not-latched shutdown function activated when a condition of mains under voltage is detected. The Brown-out comparator is internally referenced to V_{BRth} threshold, see *Table 8: "Controller section "*, and disables the PWM if the voltage applied at the BR pin is below this internal reference. Under this condition the power MOSFET is turned off. Until the Brown out condition is present, the V_{DD} voltage continuously oscillates between the V_{DDon} and the UVLO thresholds, as shown in the timing diagram of *Figure 31: "Brown-out protection: BR external setting and timing diagram"*. A voltage hysteresis is present to improve the noise immunity.

The switching operation is restarted as the voltage on the pin is above the reference plus the before said voltage hysteresis. See *Figure 5: "Brown out threshold test circuit"*.

The Brown-out comparator is provided also with a current hysteresis, I_{BRhyst}. The designer has to set the rectified input voltage above which the power MOSFET starts switching after brown out event, V_{INon}, and the rectified input voltage below which the power MOSFET is switched off, V_{INoff}. Thanks to the I_{BRhyst}, see *Table 8: "Controller section "*, these two thresholds can be set separately.

Figure 31: Brown-out protection: BR external setting and timing diagram



Fixed the V_{INon} and the V_{INoff} levels, with reference to *Figure 31: "Brown-out protection: BR external setting and timing diagram"*, the following relationships can be established for the calculation of the resistors R_H and R_L:

Equation 9

$$R_L = \frac{V_{BRhyst}}{I_{BRhyst}} + \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{V_{INoff} - V_{BRth}} \times \frac{V_{BRth}}{I_{BRhyst}}$$

Equation 10

$$R_H = \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{I_{BRhyst}} \times \frac{R_L}{R_L + \frac{V_{BRhyst}}{I_{BRhyst}}}$$

For a proper operation of this function, $V_{IN\ on}$ must be less than the peak voltage at minimum mains and $V_{IN\ off}$ less than the minimum voltage on the input bulk capacitor at minimum mains and maximum load.

The BR pin is a high impedance input connected to high value resistors, thus it is prone to pick up noise, which might alter the OFF threshold when the converter operates or gives origin to undesired switch-off of the device during ESD tests.

It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

If the brown-out function is not used the BR pin has to be connected to GND, ensuring that the voltage is lower than the minimum of V_{DIS} threshold (50 mV, see *Table 8: "Controller section "*). In order to enable the brown-out function the BR pin voltage has to be higher than the maximum of V_{DIS} threshold (150 mV, see *Table 8: "Controller section "*).

7.13 2nd level overcurrent protection and hiccup mode

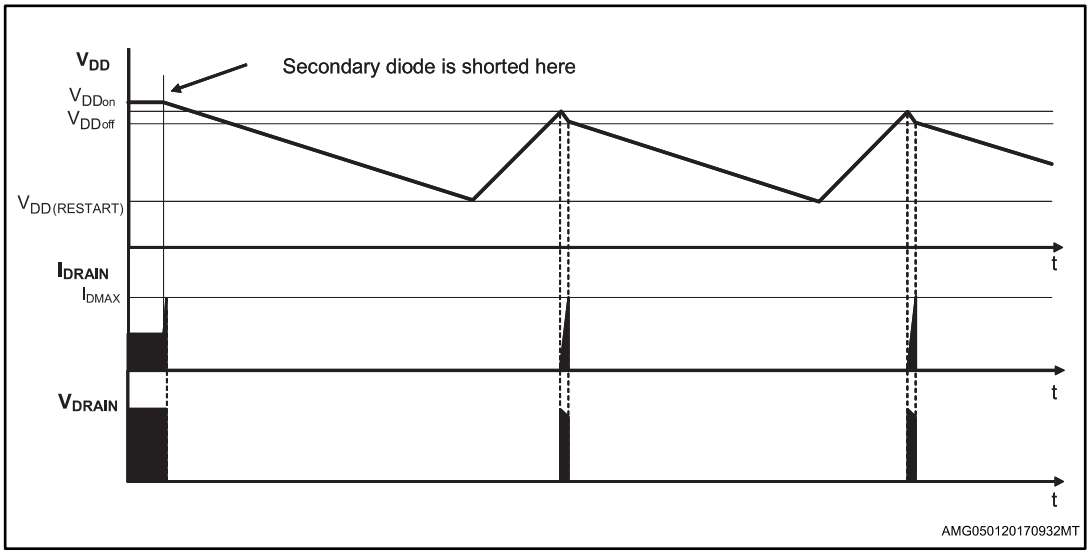
The VIPER17 is protected against short circuit of the secondary rectifier, short circuit on the secondary winding or a hard-saturation of fly-back transformer. Such as anomalous condition is invoked when the drain current exceed the threshold I_{DMAX} (see *Table 8: "Controller section "*).

To distinguish a real malfunction from a disturbance (e.g. induced during ESD tests) a “warning state” is entered after the first signal trip. If in the subsequent switching cycle the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; otherwise if the I_{DMAX} threshold is exceeded for two consecutive switching cycles a real malfunction is assumed and the power MOSFET is turned OFF.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the voltage on the V_{DD} capacitor decays till the V_{DD} under voltage threshold (V_{DDoff}), which clears the latch.

The startup HV current generator is still off, until V_{DD} voltage goes below its restart voltage, $V_{DD(RESTART)}$. After this condition the V_{DD} capacitor is charged again by 600 µA current, and the converter switching restarts if the V_{DDon} occurs. If the fault condition is not removed the device enters in auto-restart mode. This behavioral results in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. See the timing diagram of *Figure 32: "Hiccup-mode OCP: timing diagram"*.

Figure 32: Hiccup-mode OCP: timing diagram



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 SO16 narrow package information

Figure 33: SO16 narrow package outline

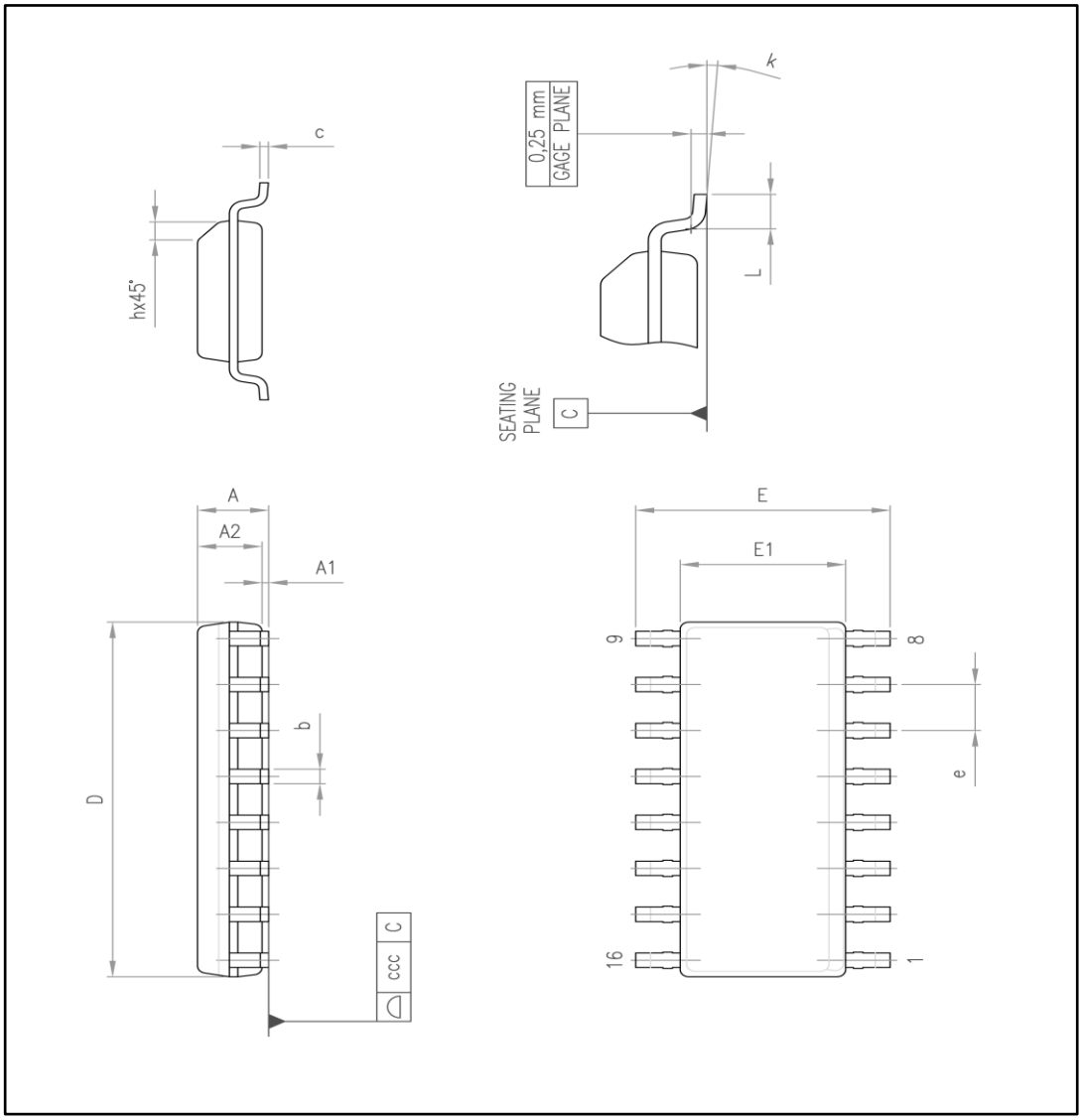


Table 10: SO16 narrow mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

8.2 DIP-7 package information

Figure 34: DIP-7 package outline

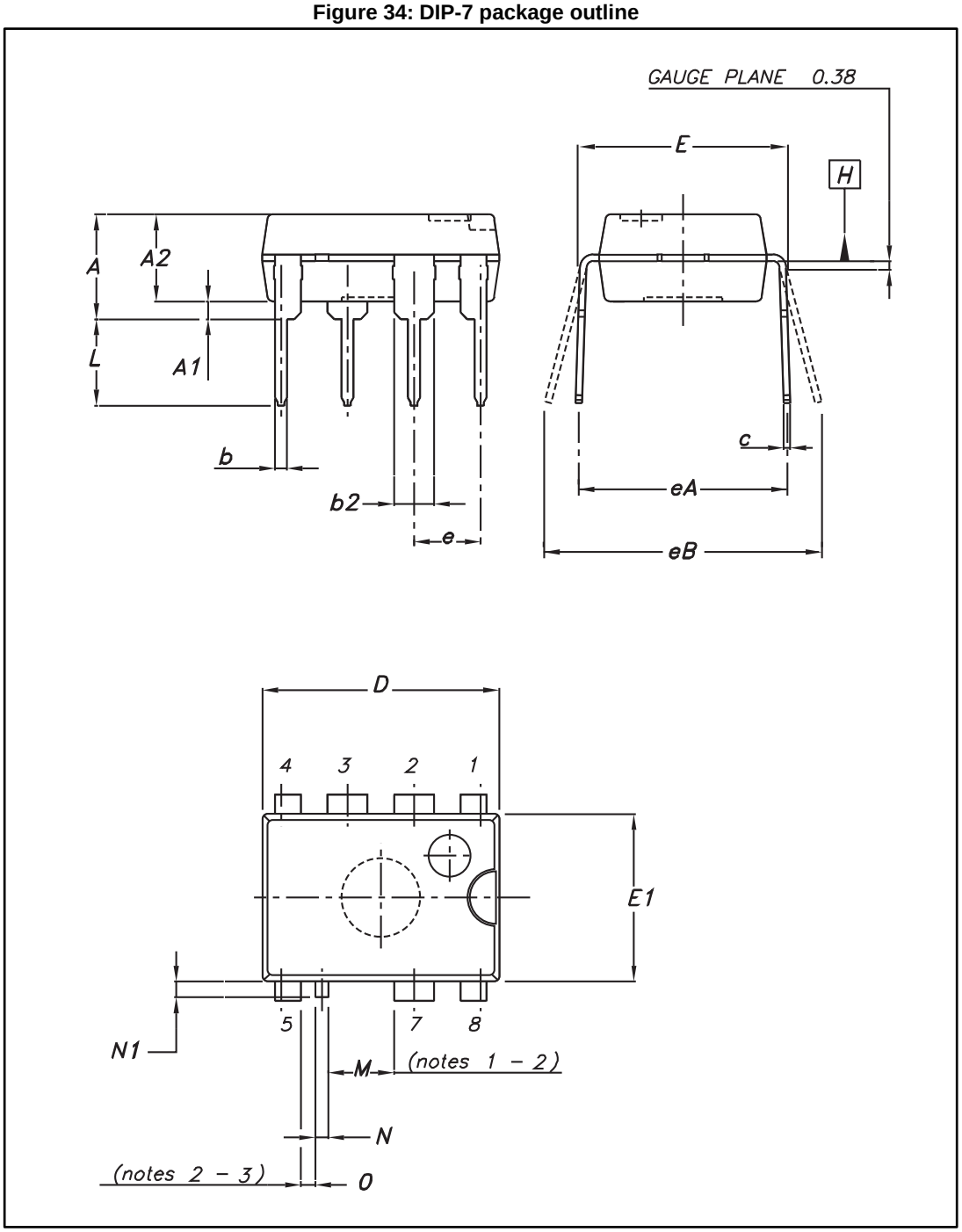


Table 11: DIP-7 package mechanical data

Dim.	mm			Notes
	Min.	Typ.	Max.	
A			5.33	
A1	0.38			
A2	2.92	3.30	4.95	
b	0.36	0.46	0.56	
b2	1.14	1.52	1.78	
c	0.20	0.25	0.36	
D	9.02	9.27	10.16	
E	7.62	7.87	8.26	
E1	6.10	6.35	7.11	
e		2.54		
eA		7.62		
eB			10.92	
L	2.92	3.30	3.81	
M[(1)(2)]		2.508		6 - 8
N	0.40	0.50	0.60	
N1			0.60	
O[(2)(3)]		0.548		7 - 8

Notes:

(1) Creepage distance > 800 V.

(2) Creepage distance as shown in the 664-1 CEI / IEC standard.

(3) Creepage distance 250 V.

General package performance

- The leads size is comprehensive of the thickness of the leads finishing material.
- Dimensions do not include mold protrusion, not to exceed 0,25 mm in total (both side).
- Package outline exclusive of metal burrs dimensions.
- Datum plane “H” coincident with the bottom of lead, where lead exits body.
- Ref. POA MOTHER doc. 0037880.

9 Revision history

Table 12: Document revision history

Date	Revision	Changes
14-Feb-2008	1	Initial release
19-Feb-2008	2	Updated: *Figure 1 on page 1, Figure 3 on page 4*
21-Jul-2008	3	Added new SO16 package
30-Sep-2008	4	Updated *Equation 9, Equation 10*
16-Jan-2009	5	Updated *Chapter 7.13 on page 27*
20-Jul-2009	6	Updated application paragraph in coverpage and *Table 8 on page 8*
14-Jun-2010	7	Updated *Figure 3 on page 4* and *Table 3 on page 4*
23-Jul-2013	8	Updated *Table 8: Controller section*. Minor text changes.
30-Aug-2013	9	Modified the footnote in *Table 8: Controller section.*
20-May-2014	10	Modified the title and the features in cover page. Updated *Section 3: Pin settings, Section 4.1: Maximum ratings, Section 4.3: Electrical characteristics.* Minor text changes.
16-Feb-2017	11	Updated *Table 5: "Thermal data"*, *Table 7: "Supply section "* and *Table 8: "Controller section "*. Minor text changes.

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VIPer17

UL39BD to UL39BG circuit modifications

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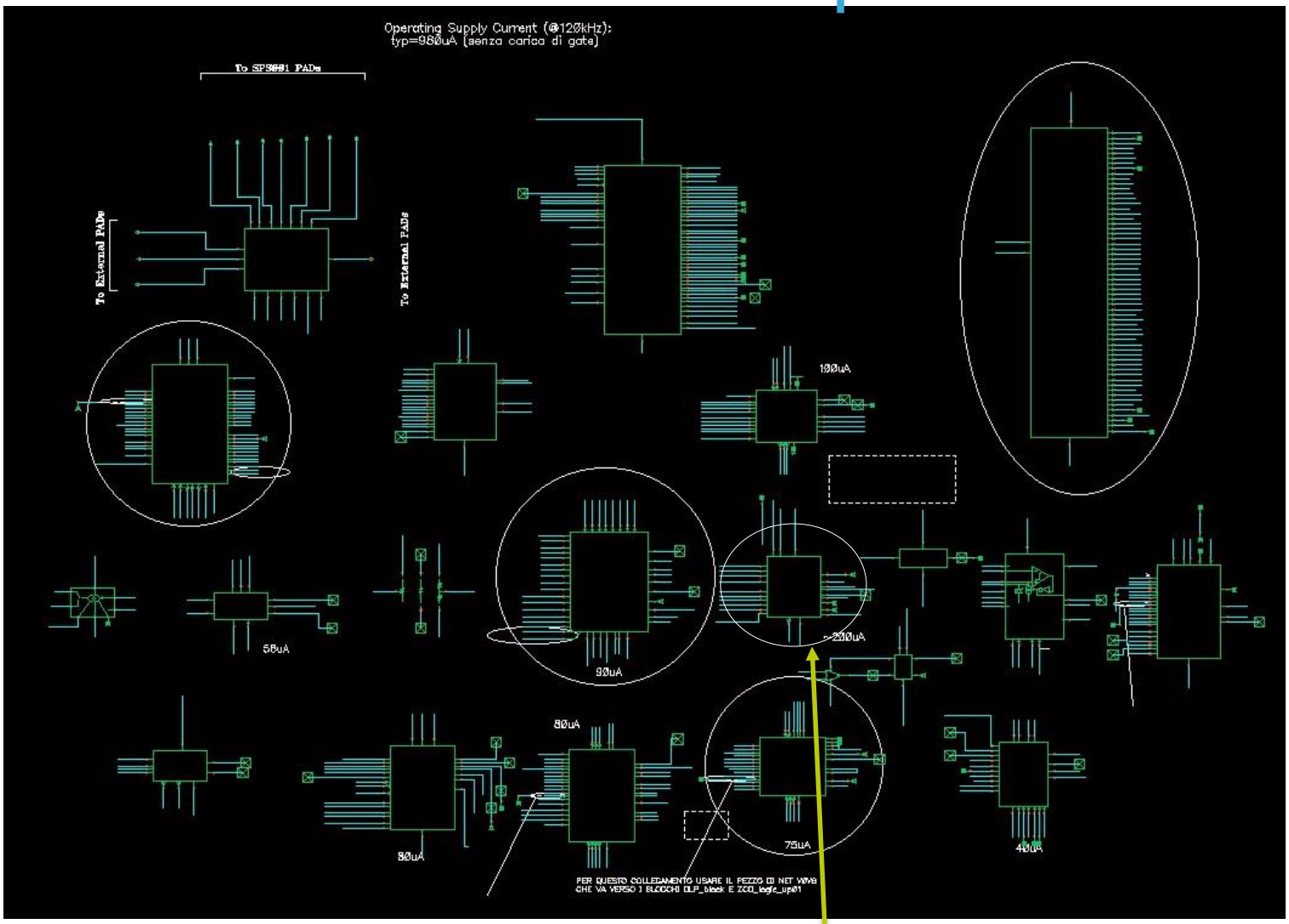
UL39BD to UL39BG

Modifications in some blocks are highlighted for:

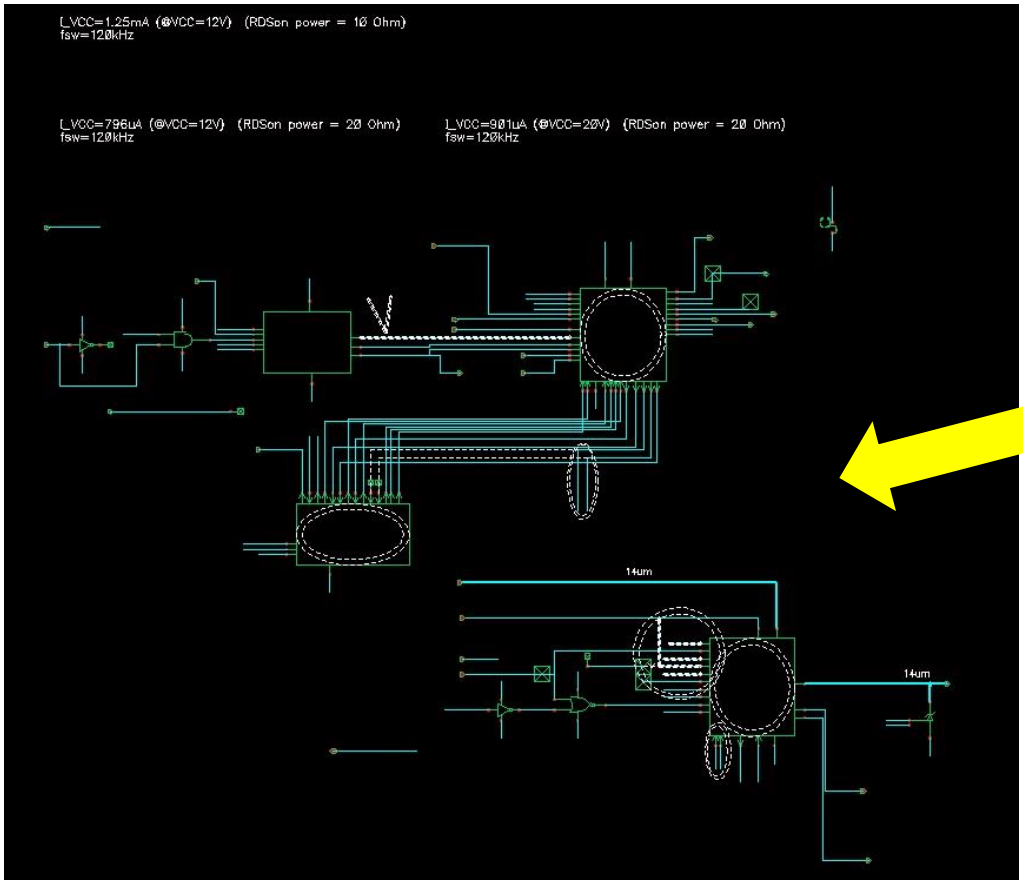
- Improving the Driver functionality against process spread and high temperature

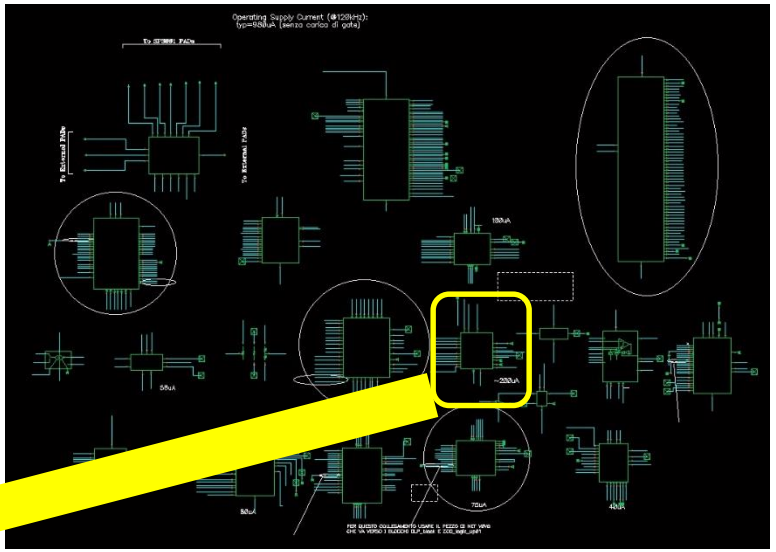
Top-level Circuit



Modified Blocks from UL39BD to UL39BG

Modified Blocks for Driver improving

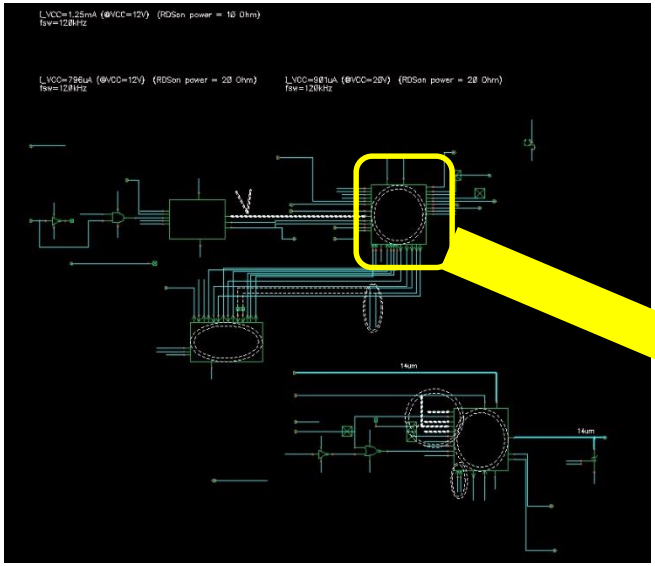


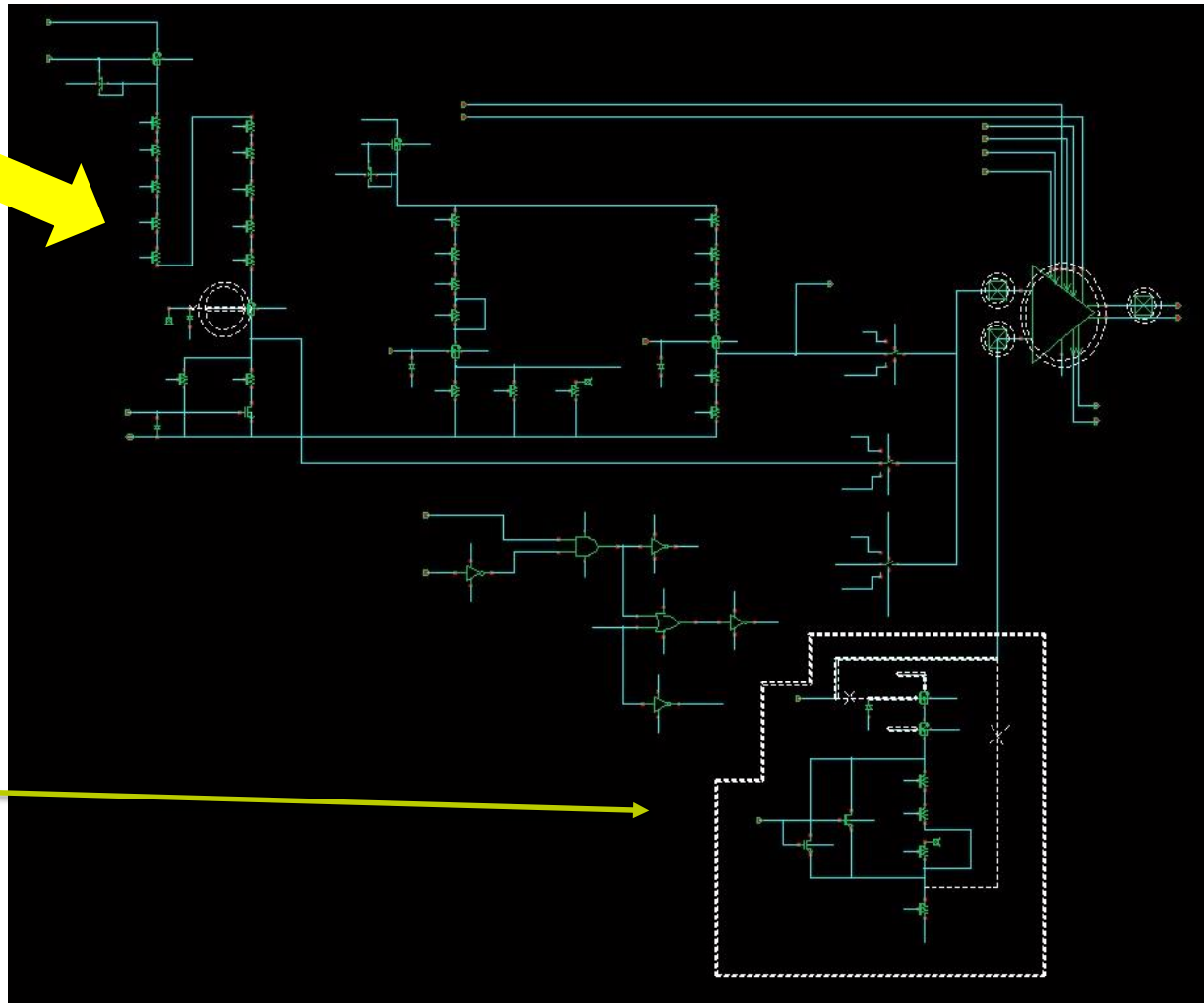


The modified blocks are:

- Driver Comparator
- Ibias of driver comparator
- Driving stage

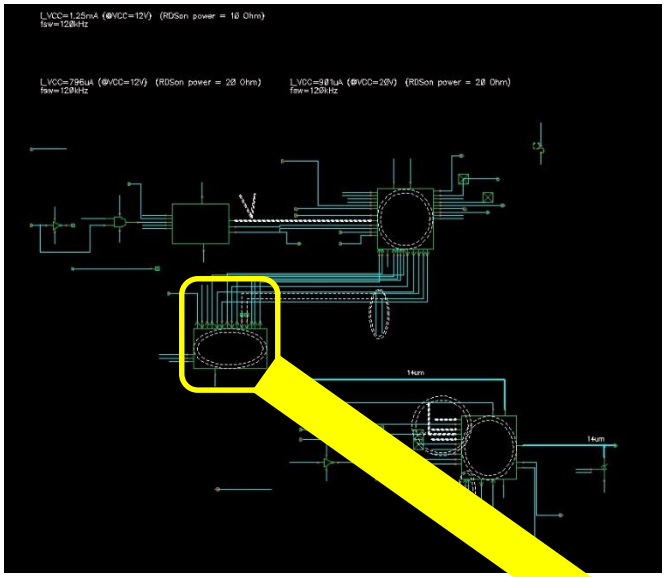
Modifications in Driver comparator



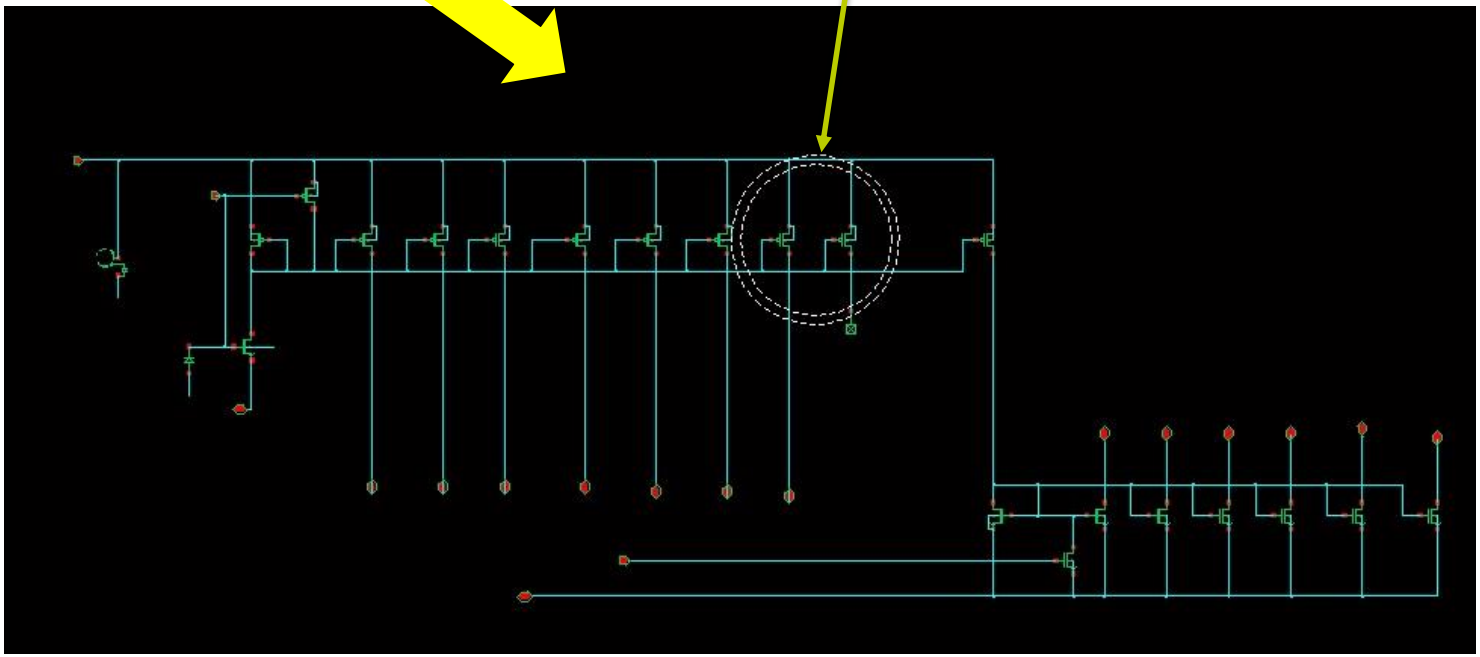


Driver comparator: some connections have been modified to improve the functioning vs process spread and high temperature

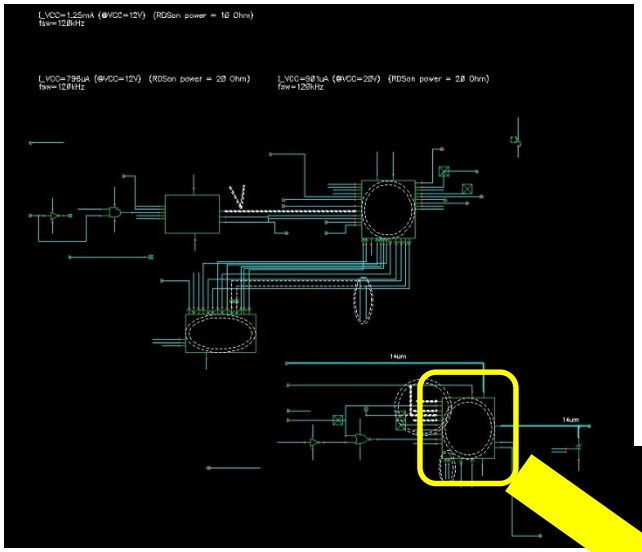
Modifications in Ibias of Driver comparator



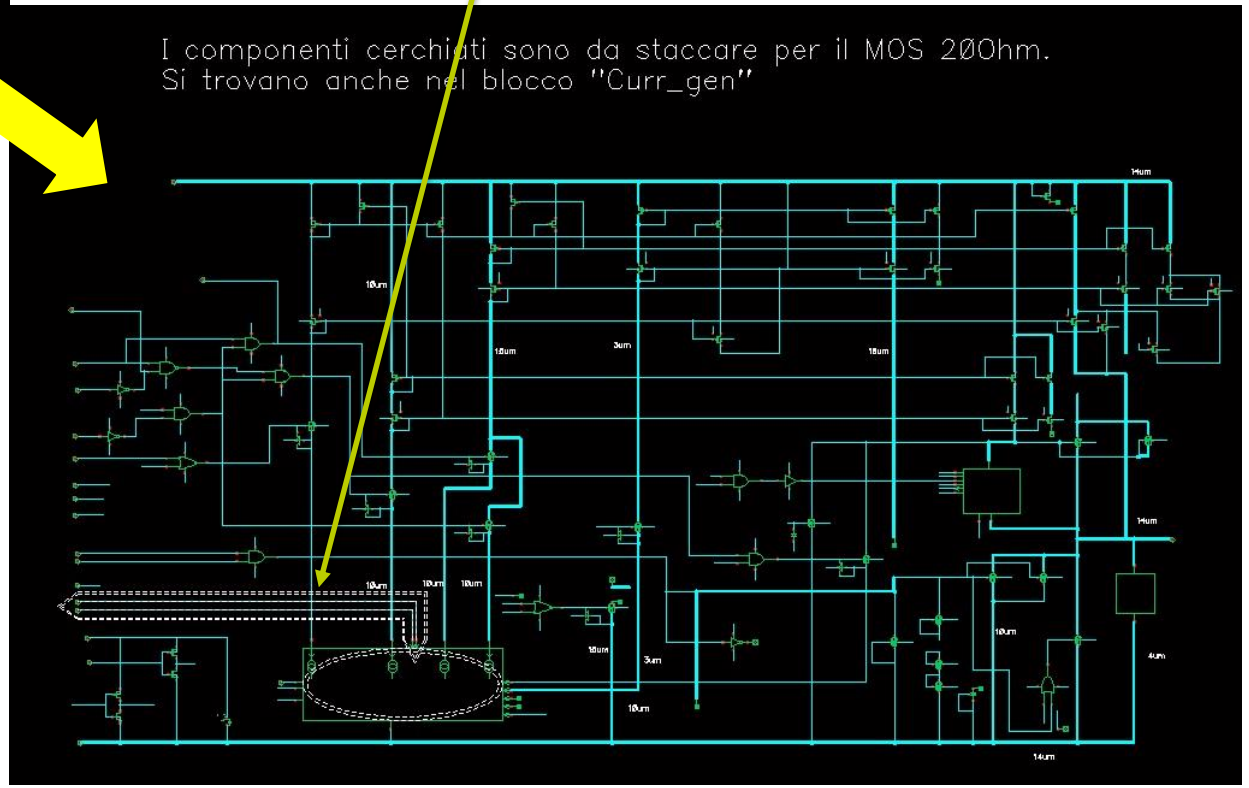
Ibias of Driver comparator: some connections have been modified to improve the functioning vs process spread and high temperature



Modifications in Driving stage



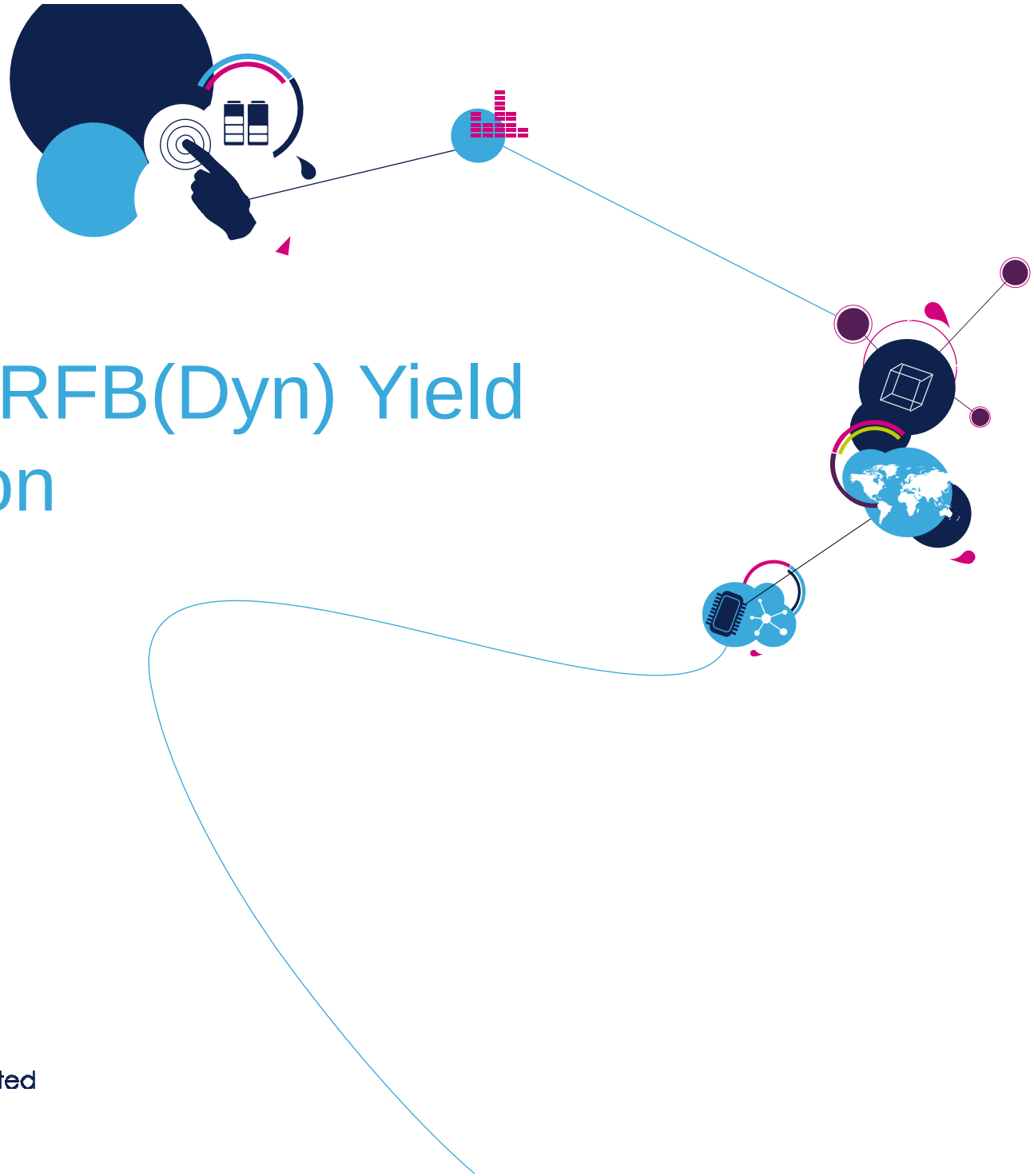
Driving stage: some connections have been modified to improve the functioning vs process spread and high temperature



UL39BD to UL39BG: Conclusion

From UL39BD to UL39BG have been done the following modifications by means Metal1, via1, metal2, via2, metal3:

- Improvement of the Driver functionality against process spread and high temperature



VIPER17 RFB(Dyn) Yield comparison

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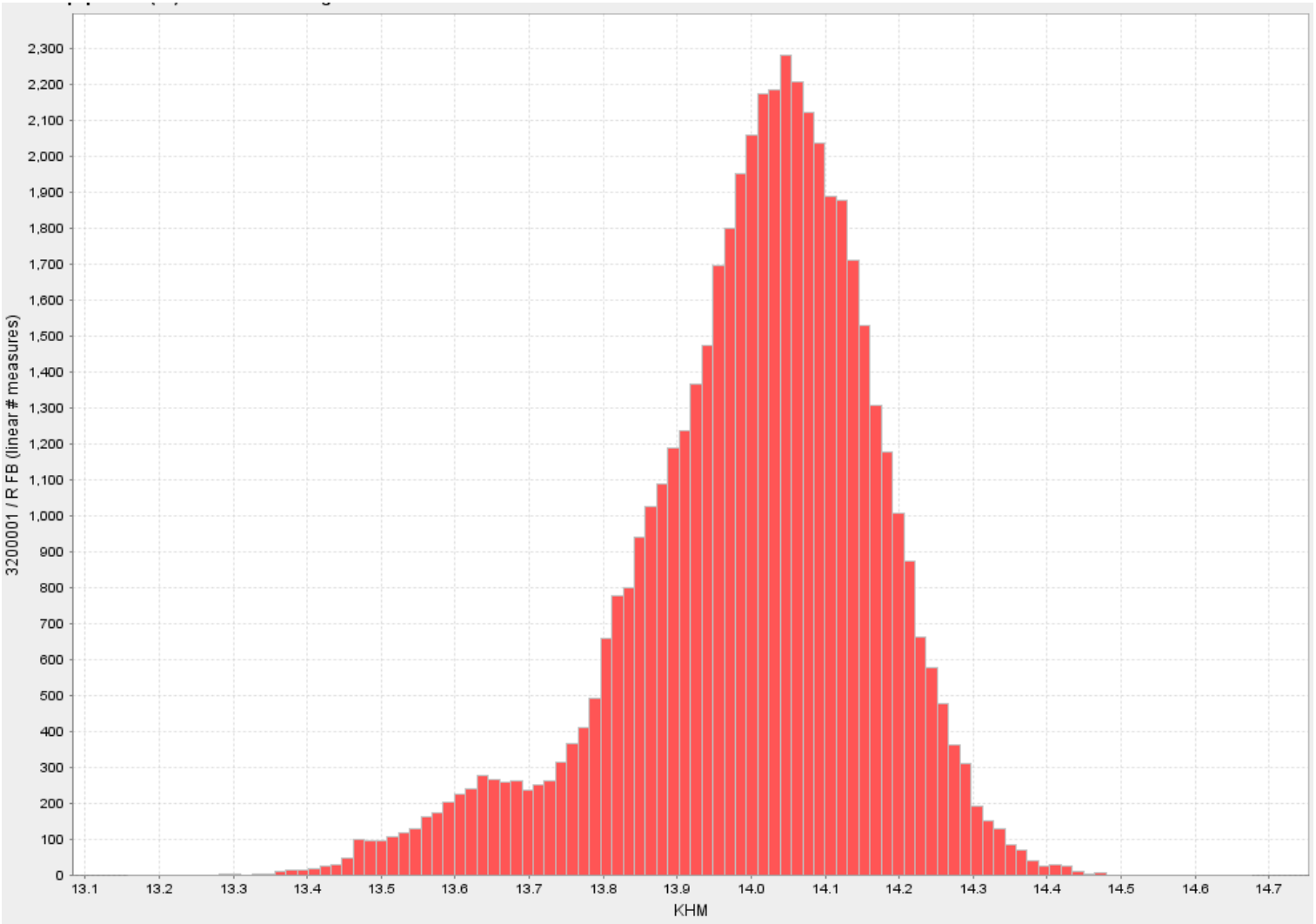
Typical RFB (Dyn) distribution



Correlation Table

RFB old limits (14 – 19) Kohm	RFB new limits (12 – 19) Kohm
Yield = 65%	Yield = 100%

Conclusion

Changing RFB (Dyn) parameter limits from 14 – 19 Kohm to 12 – 19 Kohm we increase the Final test yield according to ST standard

VIPer17(UL39BG)
HFB change validation report

Author: Claudio Mazzurco

Catania 19th December 2016

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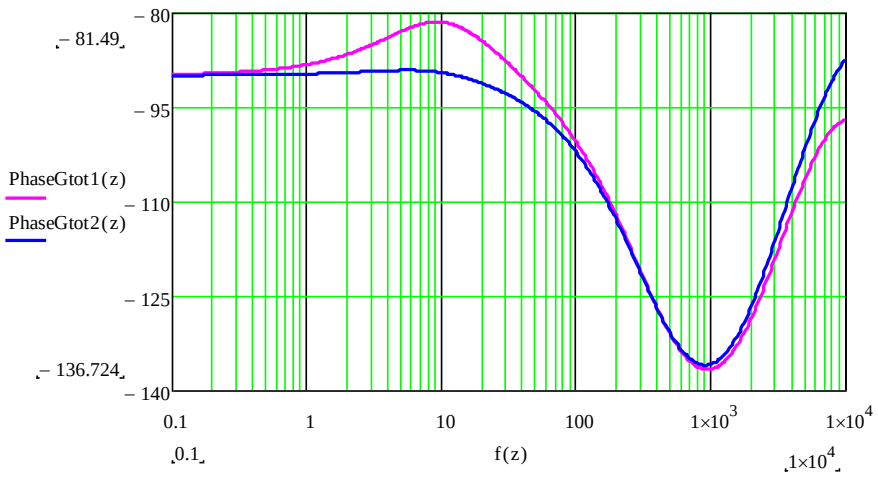
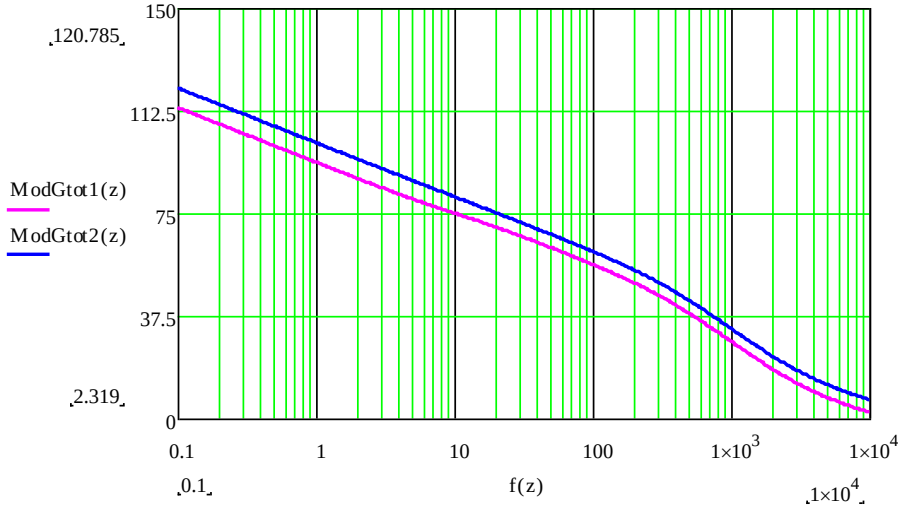
HFB issue evaluation

First of all we calculate the passive component setup by considering the standard HFB (ΔVFB / ΔID) range: 4 - 9 and choosing 6.5 value (arithmetic mean).
Below we show the phase margin and module graph calculated to achieve the desired system bandwith (the product between plant gain and compensator gain of transfer function, at $\mathbf{f_{cross}}$ = 8 kHz, was imposed equal to 1).



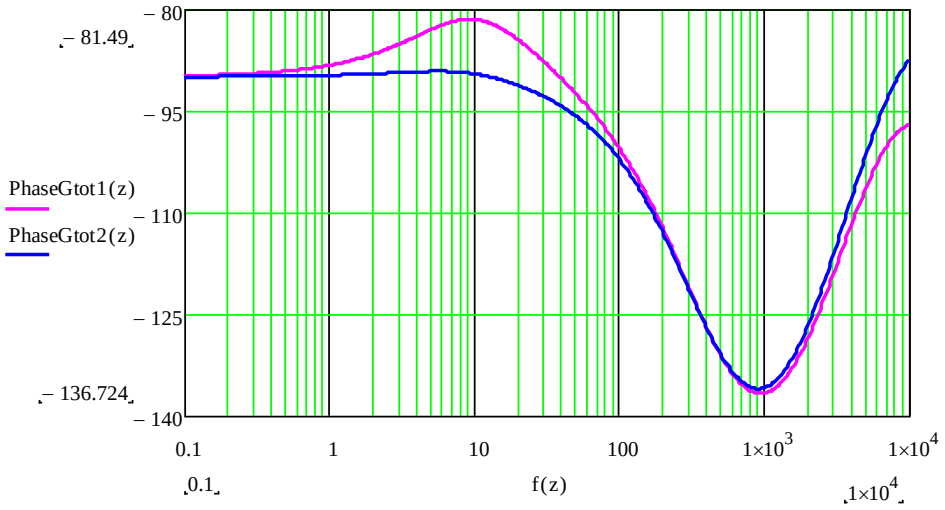


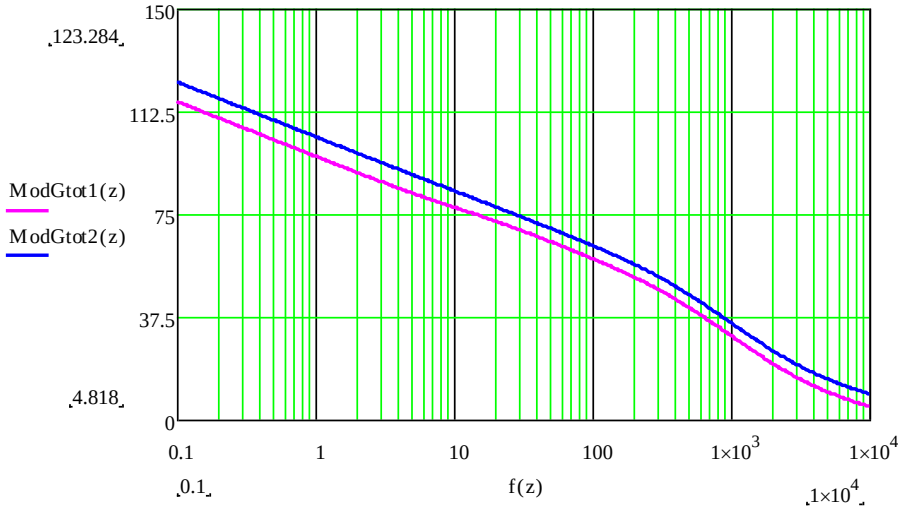
By equations we calculate the achieved $\mathbf{f_{cross}}$ and phase margin at previous low limit:

1. f_{cross} = 14.4 kHz
2. Phase Margin = 81.7 °

RFB issue evaluation

Once fixed the component setup, in other word the Bill Of Material of design, we recalculate the phase margin and the system bandwith changing the HFB with the new suggested low limit: 3.
Below the related phase margin and module graph are showed:





By equations we calculate the achieved $\mathbf{f_{cross}}$ and phase margin:

1. f_{cross} = 21.9 kHz
2. Phase Margin = 75.1 °

RFB issue evaluation
Conclusion

The HFB issue was investigated on slides number 2 and 3.
The below reassuming table, show the negligible impact of HFB drifting value against the system stability and dynamic.

	HFB = 4 (old)	HFB = 3 (new)
f_{cross}	14.4 kHz	21.9 kHz
Phase Margin	81.7 °	75.1 °

VIPer28 PIL IPD-IPC/13/7734

Fabio Salanitri

Segment Marketing S.Manager

IPG- IPD OFF LINE Bus.Unit.

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PIL IPD-IPC/13/7734
Dated 01 Mar 2013

Sales Type/product family label	see attached list
Type of change	Product design change
Reason for change	yield improvement
Description	In order to improve the yield of the VIPER28xx product, we have performed a metal mask modification on the controller UP02.
Forecasted date of implementation	22-Feb-2013
Forecasted date of samples for customer	20-Mar-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	22-Feb-2013
Involved ST facilities	Catania M5 (Italy)

T&F Yield before PIL notification

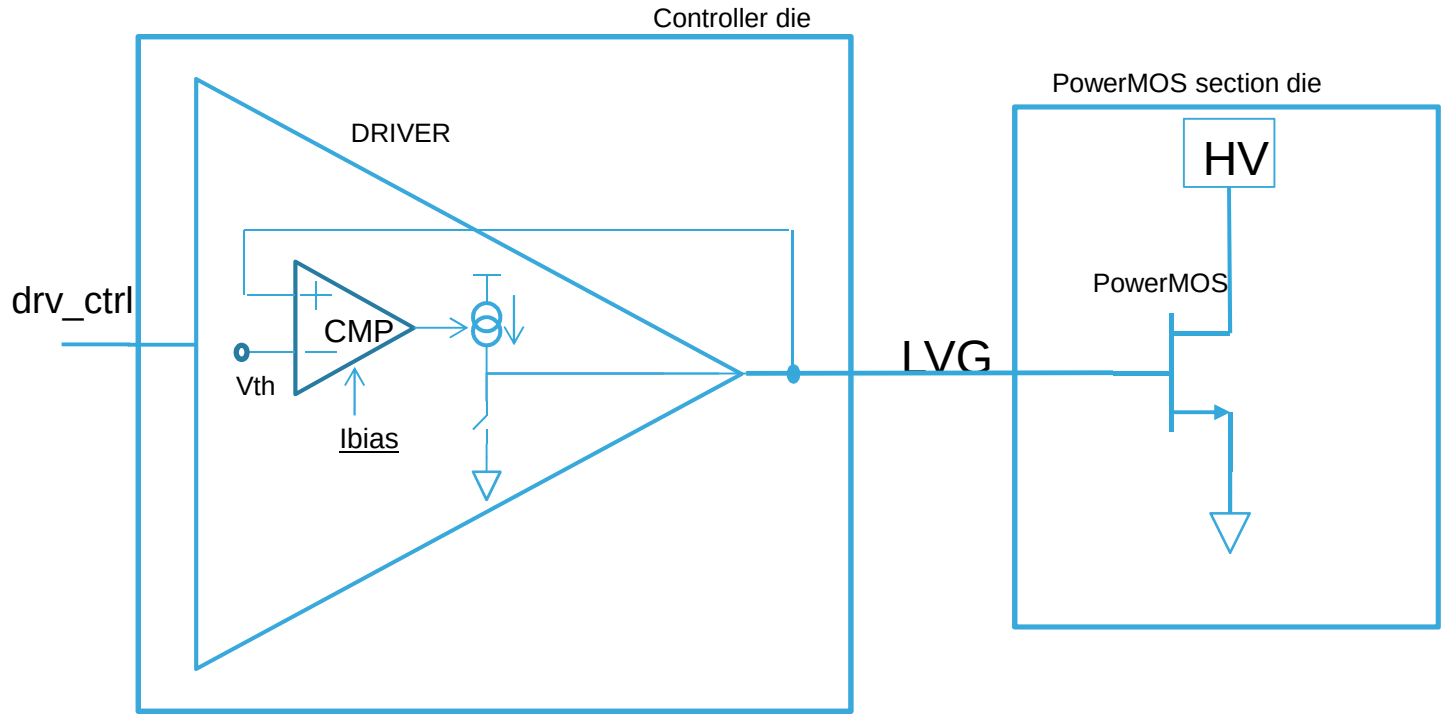
	Lot No	Product Code	TP	Normalized Yield Vs. target
BA CONTROLLER 2012	GK2090V701	VIPER28LN-2LF/	MV54LHOT	-0.777
	GK2090V7ZZ			-0.235
	GK2090V7ZY			-0.343
	GK1421AK01	VIPER28LN-2LF/	MV54LHOT	-2.849
	GK1421AM01			-2.006
	GK1421AH01			-1.537
	GK1421AD01	VIPER28LN-2LF/	MV54LHOT	-1.124

Loss of final yield at hot temperature of I_{DD1} parameter.
I_{DD1} parameter is the device current consumption when the Power MOSFET is switching

This loss of yield was unacceptable for ST back end procedure

Containment action vs I_{DD1} yield loss

- the Ibias of CMP comparator of DRIVER has been changed.
- Change has no impact form, fit, function, processing



T&F Yield after PIL notification

	Lot No	Product Code	TP	Normalized Yield Vs. target
2014	G440319K08	VIPER28LN-2LF/	MV54FHL1	0.067
	G44040DV01			0.060
	G435109Y08			0.102
	G435109Y05			0.137

Final yield at hot temperature of IDD1 parameter is within ST back end procedure

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IPD – IPC – PRODUCT RELIABILITY

Product Reliability Certificate

Line :……..……MV54 BBX(VIPER28xx)
Division :……..……IND.& POWER CONV.
Aim of the Qualification:……New version

Device construction note

DIE FEATURES		
Wafer Code	:	UP02BB5 + VZ81B3T
Diffusion Site	:	CATANIA
Wafer Diameter (inches)	:	8 inches (UP02BB5) 6 inches (VZ81)
Die Size X	:	1320µm (UP02BB5) 2640µm (VZ81)
Die Size Y	:	1112 µm (UP02BB5) 2310 µm (VZ81)
Process Technology	:	BCD6-40N 3M (UP02BB5) SUPERMESH (VZ81)
Passivation	:	SiN+Polyimide (UP02BB5) SiN (VZ81)

PACKAGE FEATURES		
Package Code Description	:	PDIP7 SO16N
Assembly Site	:	ST-SHENZEN (PDIP7) UTAC Thai Limited (SO16N)
Die Attach material	:	Ablebond 8390 (PDIP7) Ablebond 8200T (SO16N)
Bonding wire 1 material	:	Au/1mils
Bonding wire 1 diameter (mils)	:	none
Molding compound	:	Hysol MG46FAM (PDIP7) Sumitomo G605 (SO16N)
Lead / Ball / Bump solder	:	Sn (PDIP7) Ni/Pd/Au PPF (SO16N)

Ojectives:

The UP02 BB5 (included in MV54 BBX) device is a metal option of the already qualified UP02 BA5 (included in MV54 BAX) device (see RR003909CS2047). Considering that this metal change is marginal from reliability viewpoint, the positive results of the reliability trial performed on previous revision can be extended to UP02 BB5 per similarity.

Conclusion:

This certificate assures that the device MV54 BBX with the above construction notes passed the reliability evaluation and can be put in mass production from reliability point of view.

Approved by:

Author: *Gianfranco D'Angelo*
Approval: *Alceo Paratore*
Antonino Motta

PCI10244 - VIPER17 controller BG adjustable (controller change)

Product Change Information

1- What is the change?

1) **Metal mask change:**
   a. Modified the driver circuit
2) **Test program and datasheet change**
   a. Modified IDDoff test condition from VDD=5V to VDD=7V.
   b. Modified RFB(DYN) minimum value from 14kΩ to 12kΩ.
   c. Modified the test conditions of HFB parameter**;** Modified the HFB min value from 4 to 3; Modified the HFB max value from 9 to 8

Commercial Product	New Finished Good	Macro Package Description	Assy Plant
VIPER17HD	VIPER17HD-19LF/	SO16 Narrow	UTAC Thai Ltd
VIPER17HDTR	VIPER17HDTR19LF/	SO16 Narrow	UTAC Thai Ltd
VIPER17HN	VIPER17HN-21HF/	PDIP 7 - MDIP .25	Nantong Fujitsu
VIPER17LN	VIPER17LN-25HF/	PDIP 7 - MDIP .25	Nantong Fujitsu
VIPER17LD	VIPER17LD-17LF/	SO16 Narrow	UTAC Thai Ltd
VIPER17LDTR	VIPER17LDTR17LF/	SO16 Narrow	UTAC Thai Ltd

2- WHY:

Reasons for the change are listed here below:

1) **Metal mask change:**
   a. In order to avoid process spread at high temperature and improve the yield of IDD1 parameter. This is a preventive action for continuous improvement and based on the experience on other product lines with the same technology (Viper28).
2) **Test program and datasheet change:**
   a. Typo error
   b. In order to improve the yield of RFB parameter
   c. In order to improve the accuracy of the HFB measurement.

3- WHEN will this change occur?

- Engineering samples available
- Production orders are available with a lead time of 14 weeks.

4- HOW will the change be qualified?

- This change will be qualified using the standard ST procedures for quality and reliability evaluation.

5- IMPACTS OF THE CHANGE:

Form:	No change
Fit:	No change
Function:	No change

6 - APPENDICES:

1) Reliability report: VIPER17_RR004216CS6080
2) VIPer17 rev11 (datasheet)
3) VIPER17_BD_to_BG_driver modification.pdf
4) VIPER17 RFB yield improvement
5) VIPER17 HFB accuracy improvement
6) VIPer17_UL39BG_validation report_HFB.pdf (Application report)
7) VIPER28_PIL7734_IDD1 testing_report